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The principle of operation of the avalanche transistor-based Marx bank circuit: A new perspective

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The principle of operation of the transistor-based Marx bank circuit has been examined. It was experimentally observed that stage-wise increase of reverse voltage does not occur. This cannot be explained by the principle of operation understood so far. A new explanation, consistent with the experimental observations and associating current-mode second breakdown of transistors, is proposed. A few experimental observations made by earlier workers have also been justified in light of the new current-controlled mechanism. © *1998 American Institute of Physics.* [S0034-6748(98)03705-8]

I. INTRODUCTION

Avalanche transistor-based Marx bank circuits (MBCs) have been used for more than 30 years to derive kilovolt order pulses having fall times of a few nanoseconds. A number of reports[1–11] have been published over these years on the design and performance of different variants of this circuit. It appears, there is a consensus that a transistor-based MBC functions as a result of doubling, tripling and so on of the collector-emitter reverse bias (V_{CE}) at successive stages of the circuit, starting from the trigger end to the load end. Surprisingly, however, to our knowledge, none of the workers demonstrated the mechanism experimentally by actually measuring the reverse voltages across various stages of the MBC.

The purpose of this article is to report our experimental observations that stagewise addition of reverse voltages does not occur. Therefore, the mechanism of operation of the MBC believed so far is not consistent. A new mechanism involving current-mode second breakdown,[12–15] which is consistent with experimental observations is proposed. Some observations made by earlier workers have also been explained in light of this new mechanism.

II. EXPERIMENT

Figure 1 shows a five-stage MBC used in this work. The circuit employed Motorola 2N5551 n-p-n bipolar junction transistors (BJTs). Values of various circuit elements are given in the figure. A similar circuit was fabricated to drive the cavity dumper of a picosecond glass laser.[8] In the present work no effort was made to select particular pieces of 2N5551 transistors by following any specific criteria[4,5,7–11] to optimize the performance of the circuit. However, it was ensured that the circuit was operating steadily for hours at a repetition rate of 20 Hz. A large number of 2N5551s were experimented with, and the results presented here are typical ones. We, therefore, believe that the features of the circuit behavior observed are quite general. A Conel-AVR model 3005 controlled power supply was used for biasing. A HP 5454A digital storage oscilloscope (DSO), fitted with a Tektronix model P6015 high voltage probe having a nominal attenuation factor of 1000 was used to monitor and record various voltage transients. All the absolute values of voltages shown have been obtained by using this nominal value of the attenuation factor. The DSO had 500 MHz analog bandwidth and 2 giga samples/second sampling rate and an effective rise time of 700 ps in the repetitive mode in which all the measurements were done. The total response time of the probe plus DSO was 3 ns. The MBC was triggered by a Scientific model HM8035 pulse generator outputting 0 to +5 V (to 50 Ω load) rectangular pulses of 2 ns rise time at typically 20 Hz repetition rate. A block diagram of the experimental setup is shown in Fig. 2.

In the first part of the study, voltage transients were measured at different nodes of the MBC, numbered in Fig. 1, and across the load resistance R_L (V_{20} in Fig. 1) with respect to ground. The waveforms obtained are shown in Figs. 3(a) and 4(a). In the second part of the study R_L was increased to 2, 20, 200 kΩ, 1.2 MΩ, and finally to 11.6 MΩ, and the corresponding outputs across the load were monitored. It is to be noted that in each case in this part of the work the load resistance R_L was divided into two halves, and for reasons explained in the next section, voltages (V_{21} in Fig. 1) across the lower half was monitored with respect to ground. The results are shown in Figs. 6 and 7. In the third and final part of the study the amplitude of the input trigger was varied, keeping the pulse width constant at around 30 ns. The trigger voltage was changed in the range of 1.3 to 4.7 V. Outputs across a constant load R_L (1 kΩ) were recorded for supply voltages of 900 and 1000 V, and are shown in Figs. 7(a) and 7(b), respectively. In this experiment only two stages of the MBC shown in Fig. 1 were used to simplify the circuit. Further, the base terminals were kept open.

III. RESULTS AND DISCUSSIONS

Voltages measured at the collector-ends (V_3, V_7, V_{11}, V_{15}, and V_{19}) and the emitter-ends (V_4, V_8, and V_{16}) of different stages are plotted with time in Figs. 3(a) and 4(a), respectively. The waveforms contain fluctuations due to impedance mismatch between the circuit and the probe. Nu-

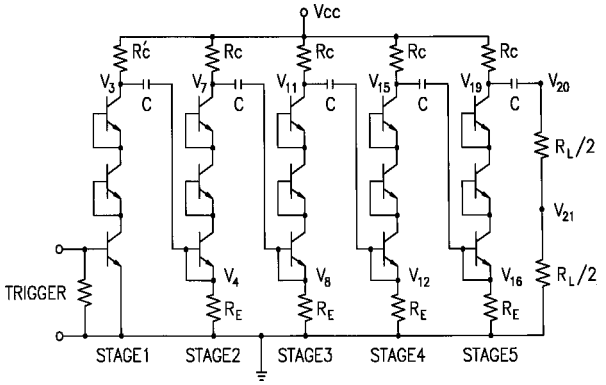

FIG. 1. The Marx bank circuit used in this work. Various node voltages measured are labeled as V_3 through V_{19}. Voltage V_{20} across the load has usually been termed as V_{R_L}. Circuit elements are $R_C'=1$ MΩ, $R_C=680$ kΩ, $R_E=680$ kΩ, $R_L=1$ kΩ, and C=471 pF. Supply voltage $V_{CC}=1000$ V.

merical fast Fourier transform (FFT) was applied to get rid of these oscillations. Results obtained by processing the data given in Figs. 3(a) and 4(a) are plotted in Figs. 3(b) and 4(b), respectively. Comparisons between Figs. 3(a) and 3(b) and Figs. 4(a) and 4(b) readily reveal that no useful information was lost in the FFT. We shall, therefore, refer to Figs. 3(b) and 4(b) for further analysis. It is found that voltages at either end of a stage falls from its corresponding pretrigger value. The important aspect to note is that within our temporal resolution the falls are simultaneous. It is not that the fall in voltage at a collector (or emitter) node of a stage is complete and only then the voltage at the collector (or emitter) node of the succeeding stage starts falling. Then the voltage across each of the stages (V_{S1} through V_{S5}) at an instant is computed by calculating the difference between the voltage at the collector-end and that at the emitter-end at the same time. The voltage across the first stage V_{S1} is simply V_3 since corresponding emitter end is grounded while voltages across other stages are $V_{S2}=(V_7-V_4), V_{S3}=(V_{11}-V_8)$ and so on. These are shown along with V_{R_L} (V_{20} in Fig. 1) in Fig. 5. It is clearly visible from Fig. 5 that reverse voltages across the second and successive stages (V_{S1} through V_{S5}) of the circuit are never doubled, tripled, etc., compared to the voltage across the first stage. Further, within the time resolution

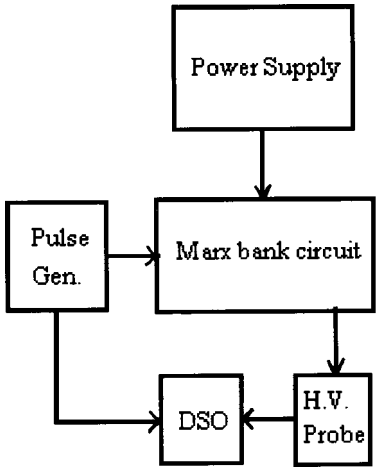

FIG. 2. Block diagram of the experimental system used in the work.

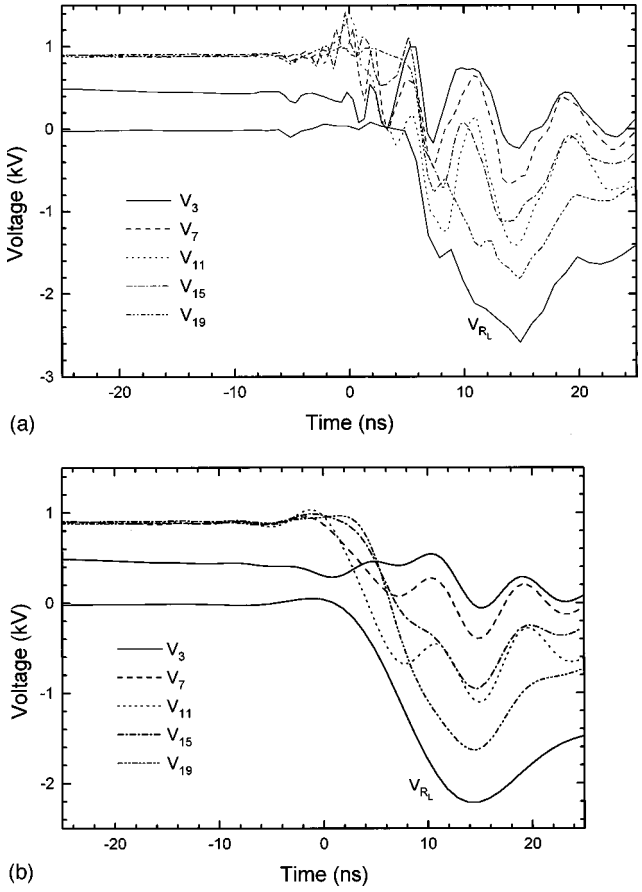

FIG. 3. (a) Voltages measured at the topmost collector terminals (see Fig. 1) of different stages of the MBC along with the load voltage, plotted against time. (b) Voltages obtained by applying numerical FFT to the data presented in (a).

of our setup, the negative output voltage pulse across the load builds up synchronously with the voltages across the transistors falling with time. This means that all the stages of the circuit are conducting together and the over-volting mechanism which implies sequential ''switching on'' of successive stages is incompatible with this observation. In this context it is interesting that several workers reported[2,7,8] that the first stage takes the maximum time to switch on while following stages take smaller and smaller times. So far, this phenomenon has been explained by arguing that successive stages are subjected to arithmetically progressing reverse voltages, which reduces the delay. However, since no stage-wise addition of reverse voltage occurs, such an explanation does not hold good. It is, therefore, apparent that the behavior of the avalanche transistor-based MBC cannot be accounted for properly by the existing model. A new approach to explain its function is presented where the circuit current, rather than overvoltages across the transistors, is the important factor.

It is well-known for quite some time that avalanche injection induced current-mode second breakdown (CMSB) in BJTs causes transitions from a high voltage, low current state to a low voltage, high current state in nanosecond order times.[12,13] It was suggested[6,9] that this mechanism was responsible for production of high voltage fast pulses using a BJT. However, the authors did not clarify exactly how

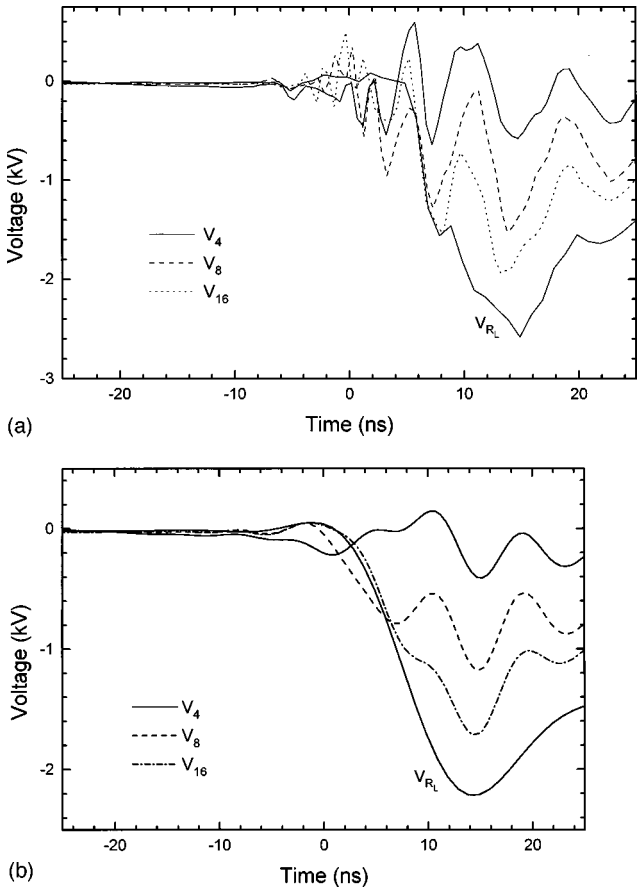

FIG. 4. (a) Voltages measured at the lowest emitter terminals (see Fig. 1) of different stages of the MBC along with the load voltage, plotted against time. (b). Voltages obtained by applying numerical FFT to the data presented in (a).

CMSB occurred in an MBC, and resorted to the idea of overvoltage. In the mechanism suggested below these aspects are taken care of.

In the quiescent condition, collector junctions of all the transistors in an MBC are biased beyond their avalanche breakdown voltage[6,7,9] BV_{CBO} or little below[1,2,4,10] BV_{CBO}. A fast-rising rectangular pulse is applied to the base of the trigger transistor to forward bias its emitter-base junction, which injects electrons to the p-type base and excess elec-

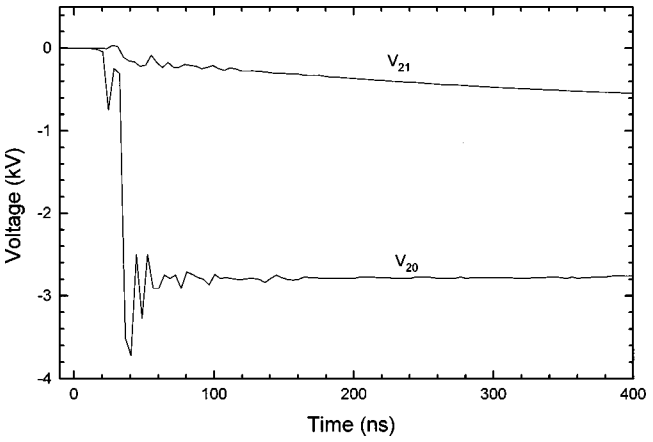

FIG. 6. Voltages across R_L (V_{20} in Fig. 1) and the lower half of the load (V_{21} in Fig. 1) with V_{CC}=900 V and R_L=1.2MΩ for the MBC shown in Fig. 1.

tron density builds up. Consequently, there is a fall in V_{CE}. This process is rather slow because the electrons in the base diffuse to the collector junction. Once in the collector, the electrons are swept out by the prevailing reverse bias, and there is a current in the external circuit. Continuity of current requires that the current exists in the entire circuit. In the subsequent transistors the current causes avalanche multiplication of carriers leading to further rise in the circuit current. In the next phase, operation of the circuit is controlled by CMSB. A critical collector-emitter voltage, V_P is required to initiate CMSB. But, V_P depends on the collector current I_C, with V_P decreasing for increasing I_C.[14,15] So, this threshold value of I_C, rather than an overvoltage, is required (for a given V_{CE}) to initiate CMSB in a transistor. The increasing circuit current pushes down the critical voltage V_P for CMSB, and at some stage CMSB is initiated. It is possible that CMSB occurs in different transistors at slightly different times, depending on individual physical parameters involved. But the current flowing through the circuit being common, it is ultimately a cooperative effect and once CMSB in initiated, voltages across all the transistors switch to low values in nanosecond order time. The amplitude and shape of the output pulse do depend on how synchronized

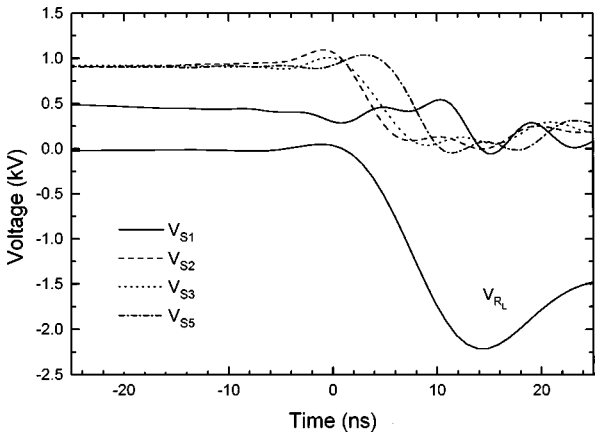

FIG. 5. Voltages across different stages of the MBC shown in Fig. 1, computed from the data presented in Figs. 3(b) and 4(b).

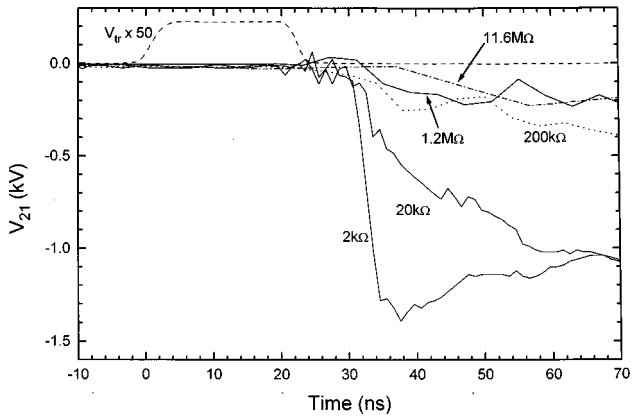

FIG. 7. Voltages (V_{21} in Fig. 1) across the lower half of the load for the various values of load resistance R_L shown in the figure. V_{tr} is the trigger pulse applied, and V_{CC}=900 V.

CMSB is in different transistors and to which levels individual voltages fall. In case all the transistors have the same avalanche breakdown voltage and equal threshold for CMSB, the amplitude of the output pulse is expected to be maximized while the fall time will be the minimum. The current-controlled mechanism of the MBC discussed so far is borne out to a large extent in Fig. 5. We see that the load current flows with voltages across different stages falling simultaneously. It is noted that unlike other stages, voltage across the first stage (V_{S1}) which contains the trigger transistor, starts falling from its quiescent value much earlier compared to voltages across other stages. This is likely to be related to the initial build-up of current following the forward bias trigger.

As a further evidence in favor of the proposed principle of operation, we refer to Figs. 6 and 7. In Fig. 6 voltages measured across R_L (V_{20}) and $R_L/2$ (V_{21}) have been plotted for $R_L=1.2$ MΩ. It is seen that V_{20} falls sharply to a large negative value, while V_{21} has a very small and gradual fall. This clearly shows that when the P6015 probe is connected to measure V_{20}, a sufficiently low-impedance path is provided to a fast falling pulse by the capacitive impedance of the probe. As a result, the threshold current for CMSB can be reached. On the other hand, when the probe is connected to measure V_{21}, a large resistance $R_L/2$ is in series with the impedance of the probe. This does not allow CMSB to occur. Keeping the above observations in mind, we may now analyze the results (see Fig. 7) of the second part of the study described in the previous section, where R_L is increased, keeping the trigger voltage and V_{CC} constant. It is observed that the output pulse (V_{21}) has a 10%–90% fall time of about 2 ns for $R_L=2$ kΩ and has an amplitude of around 1.4 kV. However, when R_L is increased to 20 kΩ, the falltime increases to around 22 ns and the amplitude decreases to about 1 kV. Similar trends continue for higher values of R_L up to 11.6 MΩ as shown in the figure. In fact, for the 11.6 MΩ load, the output pulse practically disappears. This is quite expected because, as mentioned earlier, the load resistance limits the maximum circuit-current, and a large value of R_L does not allow the current to rise to the CMSB threshold. The slowly falling low-amplitude output pulses for large R_L's may have appeared due to some relatively low-impedance alternative stray current paths which are likely to exist in such a complex circuit.

There are reports[4–6,8] of dependence of the output pulse on the nature of the applied trigger. In general, it has been observed that a hard trigger, that is, a high voltage forward bias pulse reduces the fall time of the output pulse dramatically. Also, a fast-rising long flat-top trigger shows reliable triggering while switching does not occur below some trigger amplitude.[8] We believe that triggering is a very sensitive aspect of the MBC and depends considerably on the particular piece of transistor used since the initial build-up of current occurs at this stage. In order to understand the situation systematically, the experiment described in the third part of the study was done. An MBC of only two stages was used to simplify the circuit, and to minimize the jitter in the output pulse. The base terminals of the transistors were kept open primarily to minimize the supply voltage requirement. We

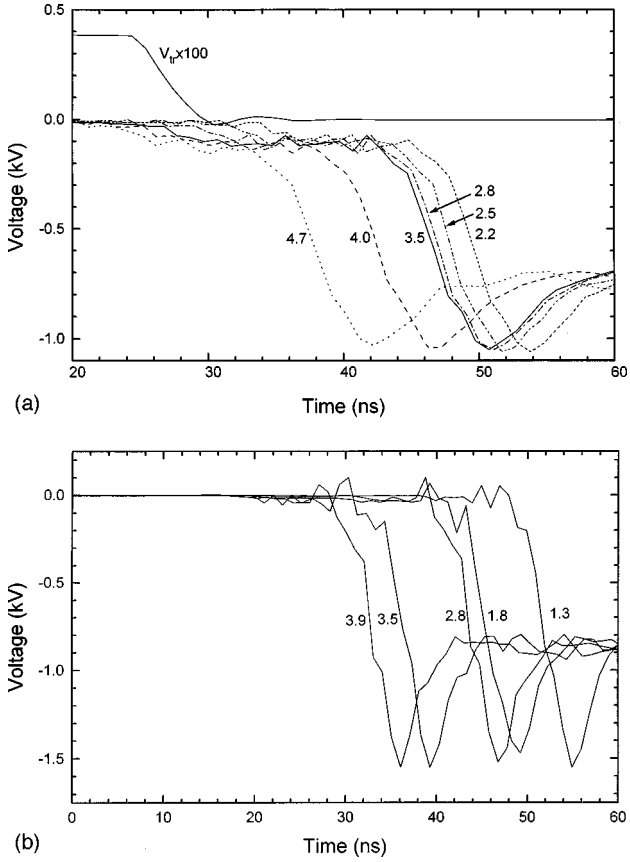

FIG. 8. Change in the output pulse V_{R_L} (V_{20} in Fig. 1) for $R_L=1$ kΩ with change in the trigger pulse (V_{tr}) amplitude for a two-stage MBC for (a) $V_{CC}=900$ V, and (b) $V_{CC}=1000$ V. Numbers associated with the curves are the corresponding trigger amplitudes in volts.

refer to Figs. 8(a) and 8(b) for a discussion of the results. In all the cases, two phases can be distinguished in the output pulse waveform. In the first phase V_{R_L} (V_{20}) falls slowly from zero while there is a fast fall in the second phase. From Fig. 7(a) we find that for $V_{CC}=900$ V, the duration of the first phase decreases from around 48 to 35 ns for a trigger pulse amplitude increasing from 2.2 to 4.7 V. Output voltages fall by 250 V in this time. During the next 4–6 ns, V_{R_L} decreases rapidly from about −250 to −900 V. A set of similar data was taken [see Fig. 8(b)] for $V_{CC}=1000$ V also. In this case the trigger voltage is varied in the range of 1.3 V to 3.9 V whereby the the first phase lasts for about 50 to 32 ns, respectively, in which output voltage falls to around −250 V. During the next 2–3 ns, V_{R_L} falls from about −250 V to −1.5 kV. In general, the output pulse appears earlier and the fall time (10%–90%) is reduced for larger trigger amplitudes. However, the trigger affects only the first part of the output pulse significantly, which may be identified with the build-up of the circuit current from a small initial value to the CMSB threshold. Longer time is supposed to be required to reach the threshold value from a smaller initial value. Once CMSB threshold is reached, the pulse falls to its minimum within a few nanoseconds, practically independent of the trigger amplitude. It is, therefore, justified that a hard trigger facilitates a faster build-up of circuit current upto the initiation of CMSB since in such a case initial current will be

high. On the other hand, a low-amplitude trigger pulse which cannot produce sufficient number of carriers to start with, is unable to trigger the MBC. However, it is difficult to prescribe any minimum limit to the trigger pulse amplitude at this stage because the phenomenon appears to be highly device specific.

We may also mention that the open-base configuration used here brings out the delay in current build-up at the initial phase more clearly compared to the case when base-emitter terminals are shorted. This is not unexpected since an open-base brings the emitter-base junction also into the process of current build-up and the junction needs to be forward biased indirectly before the CMSB threshold may be reached.

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