Electron transport in copper phthalocyanines

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Charge transport in copper phthalocyanine (CuPc), partially fluorinated CuPc (F_4CuPc), and fluorinated CuPc (F_{16}CuPc) based organic thin film transistors is studied using dual SiO_2/polymethylmethacrylate gate dielectrics. We demonstrate the strong influence of air/moisture induced electron traps on electron transport when the lowest unoccupied molecular orbital is close to the vacuum irrespective of hydroxyl-free dielectrics used in the devices. © *2010 American Institute of Physics*. [doi:10.1063/1.3284938]

I. INTRODUCTION

Electron transport in organic semiconductors is an important topic which is of fundamental academic interest and also relevant in the further development of organic electronics. Organic semiconductors, when used as active layers in field-effect devices, can, in principle, transport both carrier types.[1] However, in practical devices, very often, one of the charge carrier types is trapped. Thus, we frequently use the terms "*n*-channel materials" or "*p*-channel materials" when speaking of typical organic thin film transistor (OTFT) semiconductors. This anomaly in conductivity type (in which one carrier type is trapped despite the ability of the material to transport it) was first described by Ostrick *et al.*[2] The work of Chua *et al.*[3] showed that this trapping of one of the carrier types occurs at the interface with the gate insulator and that the use of appropriate insulators can mitigate the extent of this trapping.

In this article, we show that ambiploar transport resulting from the use of modified semiconductor-insulator interfaces works only in inert ambient (with very little oxygen and moisture) and that the most important criterion for determining the type of carrier that a material transports is the energy levels of the lowest unoccupied molecular orbital (LUMO) and highest occupied molecular orbital (HOMO). The nature of the ambient, which can influence trapping, is also an important factor which influences the charge transport in OTFT devices. Charge trapping at the organic semiconductor-dielectric interface can be minimized by suitable choice of gate dielectrics, which reduces the trap concentration at the semiconductor-insulator interface.[1,3–5] The commonly used SiO_2 dielectric is known for its electron trapping properties.[4] Organic semiconductors, such as N,N'-bis(n-octyl)-(1,7&1,6)-dicyanoperylene-3,4:9,10-bis(dicarboximide) (PDI-8CN_2),[6,7] and fluorinated copper phthalocyanine (F_{16}CuPc),[8] having sufficiently low LUMO energy levels have shown good electron transport in combination with SiO_2 as gate dielectric in ambient conditions. Yoon *et al.*[9] and Anthopoulos *et al.*[10] have shown that the electron transport in organic semiconductor with LUMO >4 eV is less affected by electron trapping. Air and moisture induced traps are a source of electron trapping and is a major problem in electron transport in many organic semiconductors.[7,11,12] We also demonstrate with the phthalocyanine (PC) system that the modification of organic semiconductor-dielectric interfaces improves the electron transport but is still limited to inert conditions.

In order to investigate the role of HOMO and LUMO energy levels on charge transport in organic semiconductors, we have chosen copper phthalocyanine (CuPc), partially fluorinated CuPc (F_4CuPc) and F_{16}CuPc as representative materials. PCs have been used as semiconductors in OTFTs, organic photovoltaic devices, organic based chemical sensors and organic light emitting devices. Fluorination of CuPc has been known to lower the HOMO and LUMO levels and change the charge transport from holes to electrons.[8] For example, CuPc and hexadecafluoro CuPc (F_{16}CuPc) have hole and electron mobility of 0.04 $cm^2/V\,s$ (Ref. 13) and 0.03 $cm^2/V\,s$,[8] respectively, and are widely used materials as hole transporting and electron transporting semiconductors, respectively. F_4CuPc has HOMO and LUMO energy levels that lie in between those of CuPc and F_{16}CuPc, and presents an interesting case to investigate charge transport using common dielectrics, and source and drain contacts. We emphasize that the CuPc/F_4CuPc/F_{16}CuPc is a model system that can be used to study the interplay between energy levels, charge transport, contacts etc. In this article, device performances with different dielectric/organic semiconductor interfaces in both air and dry nitrogen (inert) ambients and different charge carrier injecting contacts have been studied and the results described. Our study demonstrates that the nature of charge transport in organic semiconductors primarily depends on the LUMO and HOMO of organic molecules. Although suitable dielectric/organic semiconductor interfaces can induce or enhance electron transport in organic semiconductors with a LUMO level close to vacuum, this

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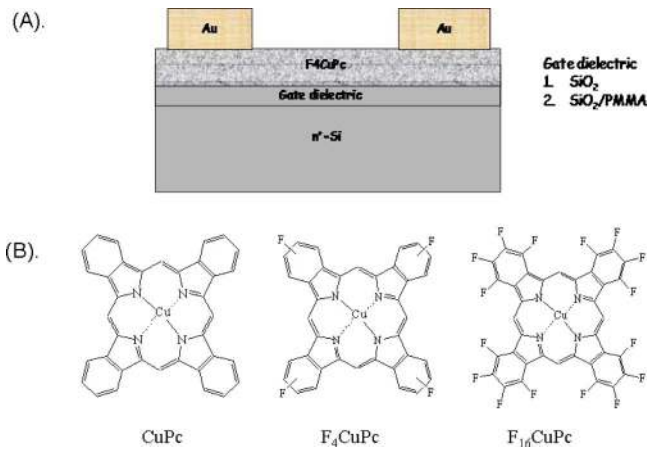

FIG. 1. (Color online) (a) Schematic structure of top contact OTFT used in study, (b) Molecular structure of CuPc, F_4CuPc,.and F_{16}CuPc molecules.

effect is limited to inert ambient conditions. The electron transport in such OTFT devices becomes suppressed significantly once devices are exposed to air and moisture which can only be partly recovered after annealing in vacuum or nitrogen.

II. EXPERIMENTAL PROCEDURE

The schematic device structures of OTFT used in the study and chemical structures of CuPc, F_4CuPc, and F_{16}CuPc are shown in Figs. 1(a) and 1(b), respectively. A heavily doped n^+-Si was used as a gate electrode with 200 nm thermally grown SiO_2 layer on top as gate dielectric. For devices with bilayer dielectrics of polymethylmethacrylate (PMMA)/SiO_2, PMMA (MW:995 K, Aldrich) was spun on Si/SiO_2 substrates at 5000 rpm for 60 seconds from 10 mg/ml solutions in toluene. After spinning, substrates were cured at 100 °C for 1 h. The organic semiconductor thin films of CuPc, F_4CuPc, and F_{16}CuPc were vacuum deposited under a base pressure of $\sim 7\times 10^{-6}$ mbar at room temperature. The film thickness (~35 nm) and deposition rate (0.03–0.05 nm/s) were measured by a quartz crystal microbalance thickness monitor. Finally, gold (Au) and aluminum (Al) source and drain electrodes (100 nm) were vacuum deposited through a shadow mask with channel length and width of (50, 100 μm) and 3 mm, respectively. The OTFTs were characterized using three-channel Keithley 4200 voltage-current source/measure system. All the device fabrication and measurements were carried out in a glove box under N_2. In order to study the effect of air/moisture on the nature of charge transport we exposed the devices to room ambient conditions for *x* hours and measured the device characteristics in air. After this, the devices were reintroduced into the glove box and were characterized again. In the next steps, devices were annealed at 100 °C for 15 min and characterized again to determine the extent of recovery from the air, air/moisture exposure.

The x-ray diffraction and atomic force microscopy (AFM) images were obtained for 35 nm F_4CuPc film on Si/SiO_2 substrate following similar growth conditions as for OTFT fabrication. PANalytical X'PERT PRO system with Cu $K\alpha$ x-ray source and molecular Imaging Veeco Metrology digital instrument microscope was used for x-ray diffraction and AFM imaging, respectively.

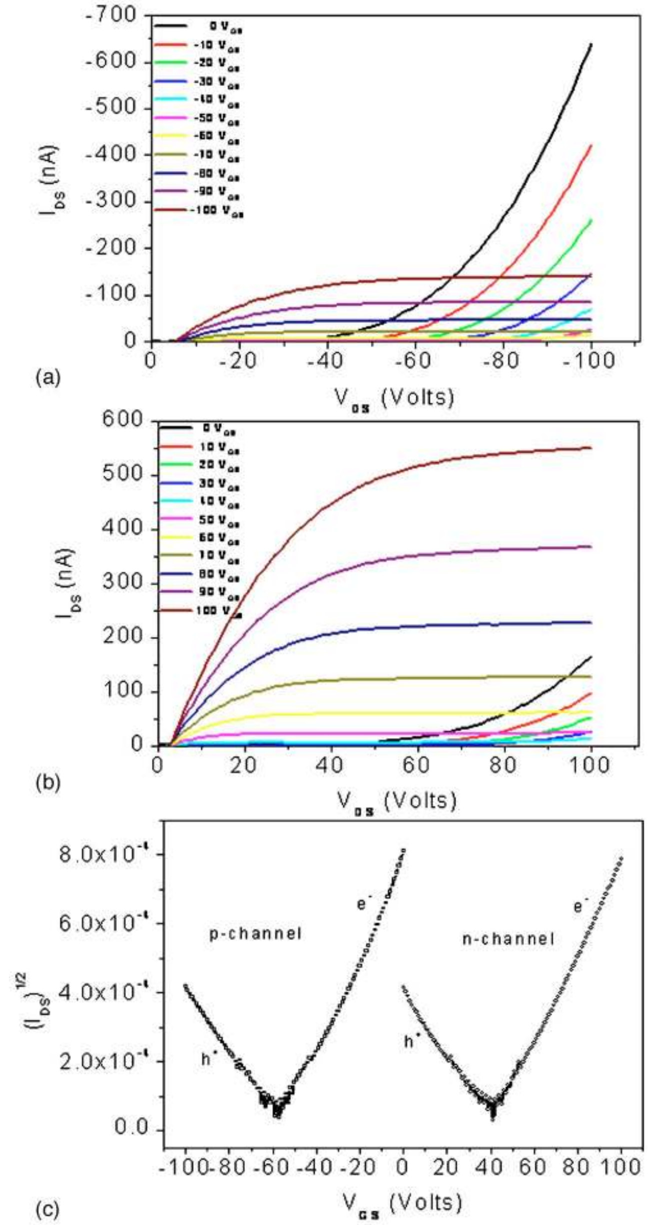

FIG. 2. (Color online) Current-voltage characteristics, (a). I_{DS}-V_{DS} (*p*-channel), (b). I_{DS}-V_{DS} (*n*-channel), and (c). I_{DS}-V_{GS}, of F_4CuPc based OTFT (L:50 μm; W: 3 mm) on SiO_2/PMMA gate dielectric.

III. RESULTS AND DISCUSSION

Figures 2(a) and 2(b) show typical drain current-voltage (I_{DS}-V_{DS}) characteristics for F_4CuPc OTFTs having PMMA/SiO_2 as gate dielectric, operating in hole and electron enhancement modes, respectively. In both operational regimes, gate bias (V_{GS}) dependent ambipolar I_{DS}-V_{DS} characteristics are observed. In Fig. 2(a), for negative V_{DS} and V_{GS}, and when $(V_{GS}-V_T)$ is positive, the effective gate voltage is positive across the channel and the OTFT current is entirely due to electron current injected from the drain. When $V_{DS}<(V_{GS}-V_T)<0$, holes are injected from source and contribute to the total drain current. In this regime, the transistor is ambipolar. When $(V_{GS}-V_T)<V_{DS}<0$, the current is almost entirely hole current and the OTFT shows typical unipolar characteristics with saturation behavior due to pinch-off mechanism in the channel. Similarly, when V_{DS} and V_{GS} both are positive [Fig. 2(b)], initially when $(V_{GS}-V_T)$ is negative, the effective gate voltage across the channel is negative and the I_{DS} current is mainly due to holes injected from the drain. For large V_{DS} and small V_G, we have an ambipolar regime with both electron and hole current. At large V_{GS}, the total drain current is dominated by electron current and the transistor exhibits linear and saturation regimes, similar to a unipolar *n*-channel TFT device.

The transfer characteristic of devices operated in hole and electron enhancement modes are shown in Fig. 2(c). In both operational modes, the highest electron currents are larger than the highest hole currents in F_4CuPc OTFTs possessing PMMA/SiO_2 as gate dielectric.

The I_{DS}-V_{DS} characteristic in hole enhancement mode, electron enhancement mode, and transfer characteristics of F_4CuPc OTFTs having SiO_2 as gate dielectric are shown in Figs. 3(a)–3(c), respectively. The observed I_{DS}-V_{DS} and I_{DS}-V_{GS} characteristics in both operational modes shows largely unipolar *p*-channel OTFT behavior. However, the transfer characteristic in hole enhancement mode [Fig. 3(c)] does indicate a small degree of electron transport.

The field-effect hole mobility $(1.2\times10^{-4}\ \text{cm}^2/\text{V s})$ and electron mobility $(3.5\times10^{-4}\ \text{cm}^2/\text{V s})$ for the ambipolar OTFT were estimated from $\sqrt{I_{DS}}$ versus V_{GS} characteristic in the saturation region as shown in Fig. 2(c). The devices having CuPc and F_{16}CuPc as active layers on SiO_2 dielectrics possessed a hole mobility of $4.7\times10^{-3}\ \text{cm}^2/\text{V s}$ and electron mobility $6.4\times10^{-3}\ \text{cm}^2/\text{V s}$., respectively. The CuPc based OTFTs on PMMA/SiO_2 dielectric exhibits weak electron transport in addition to dominant hole transport, as shown in Fig. 4(a). The ambipolar characteristic observed in CuPc based OTFTs is mainly due to a reduction of electron traps at organic/dielectric interface.

To study the effect of air and moisture on electron transport, we exposed the CuPc, F_4CuPc, and F_{16}CuPc based devices to room ambient conditions, and tested the devices, and then again reintroduced them back into the N_2 filled glove box for further testing. The electron transport in CuPc and F_4CuPc devices having PMMA/SiO_2 dielectric is completely suppressed by air/moisture exposure as shown in Figs. 4(b) and 4(d), respectively. The transfer characteristic of F_4CuPc devices before exposing to air are shown in Fig. 4(c). It clearly shows that a lesser degree of electron trapping occurs at the organic/dielectric interface due to a thin PMMA layer, and air/moisture induced electron traps stalls the electron transport almost completely. But in the case of F_{16}CuPc where the LUMO level is lowest among PCs studied here, electron transport remains substantially unaffected, although the threshold voltage of air-exposed devices becomes higher.

Annealing of air/moisture exposed devices at 100 °C in the N_2 filled glove box results in significant recovery of electron transport in F_4CuPc based devices, as shown in Fig. 4(d). The annealed devices possess about one order of magnitude higher electron current as compared to air/moisture exposed devices; however, the electron currents are still one order of magnitude lower than the electron current in pristine devices measured in the glove box under N_2. On the other hand for F_{16}CuPc devices, annealing of air/moisture exposed devices does not result in any substantial changes.

The role of injection on electron contacts is investigated using aluminum (Al) as source and drain contacts for PCs based transistors. The transfer characteristics of CuPc based transistors on SiO_2 and PMMA/SiO_2 gate dielectrics for gold and aluminum as injecting contacts are shown in Fig. 5. The aluminum source and drain contacts facilitates electron transport to some extent in CuPc based transistors on SiO_2 gate dielectrics due to lower work function of aluminum (4.1 eV) as evident in Fig. 5(b) while devices with gold injecting con-

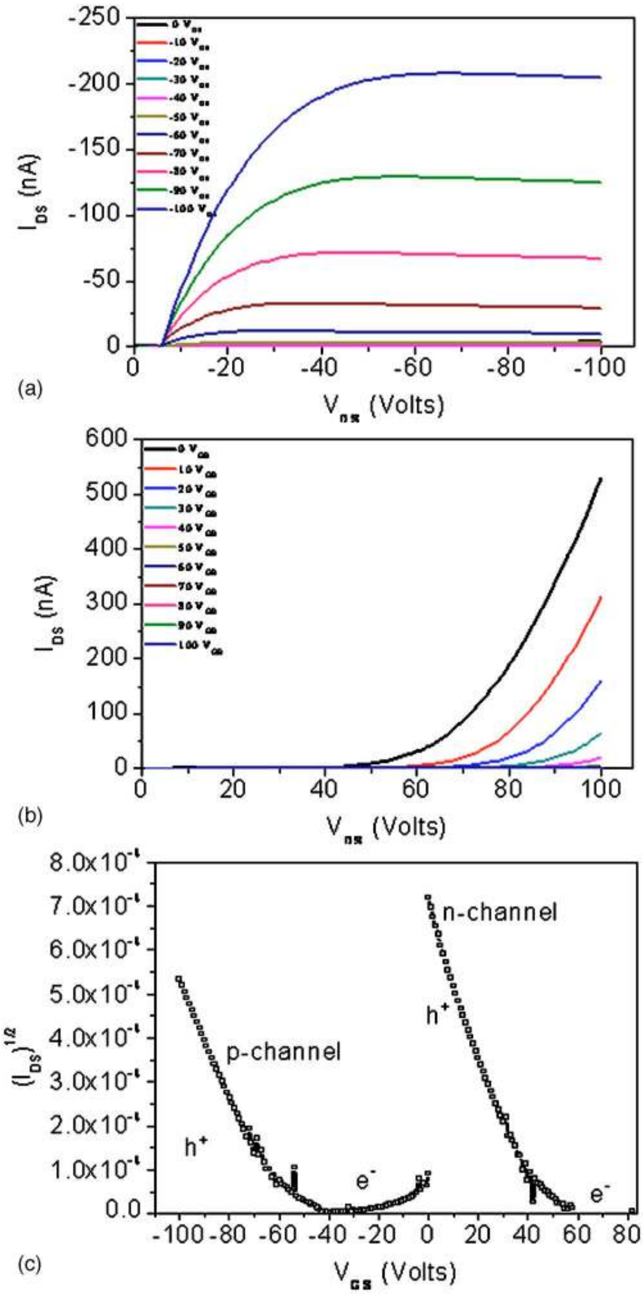

FIG. 3. (Color online) Current-voltage characteristics. (a) I_{DS}-V_{DS} (*p*-channel), (b) I_{DS}-V_{DS} (*n*-channel), and (c) I_{DS}-V_{GS}, of F_4CuPc based OTFT (L: 50 μm; W: 3 mm) on SiO_2 gate dielectric.

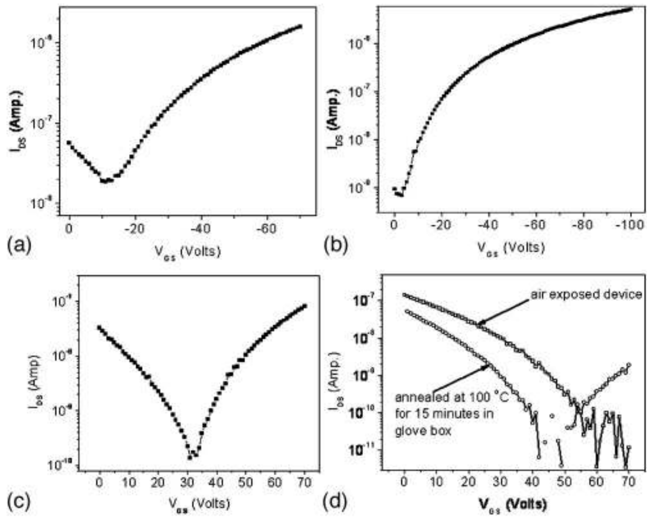

FIG. 4. Transfer characteristic of CuPc based OTFT (L: 100 μm; W: 3 mm) on PMMA/SiO_2 gate dielectric (a) before and (b) after air exposure measured in glove box under N_2. (c) and (d) shows transfer characteristic of F_4CuPc based devices before, and after air exposure, respectively. Annealing of air exposed devices at 100 °C (15 min) in the N_2 filled glove box results in significant recovery of electron transport shown in (d).

tacts shows hole transport only. For transistors on PMMA/SiO_2 gate dielectric having aluminum source and drain contacts electron current does not improve much as compared to that for transistors having gold source and drain contacts as evident in Figs. 5(c) and 5(d). On the other hand hole current of CuPc transistors on SiO_2 gate dielectric having aluminum as injecting contacts reduced to half, and by two orders of magnitude for transistors on PMMA/SiO_2 gate dielectric as compared to hole current of CuPc based transistors having Au as source and drain contacts on respective gate dielectrics. The lowering of hole current in transistors with aluminum injecting contacts is understandable due to increased hole injection barrier.

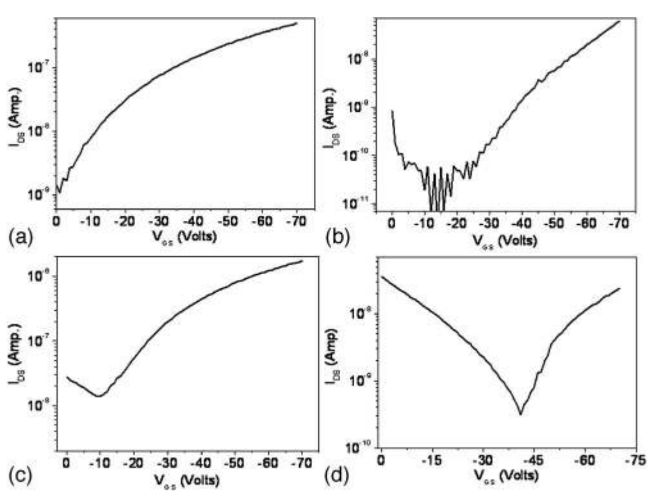

FIG. 5. Transfer characteristic of CuPc based transistors (L: 100 μm; W: 3 mm) having injecting contact metal (a). Au and (b) Al on SiO_2 gate dielectric, and (c). Au and (d). Al on PMMA/SiO_2 gate dielectric.

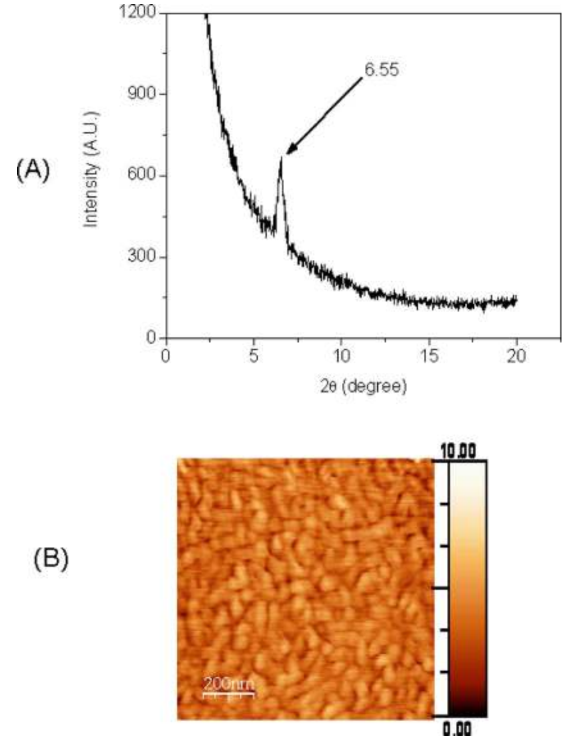

FIG. 6. (Color online) (a) X-ray diffraction pattern and (b) AFM image of F_4CuPc thin film deposited at room temperature on Si/SiO_2 substrate.

The thin film properties of F_4CuPc are similar to those of CuPc and F_{16}CuPc. Structural and morphological investigations of F_4CuPc thin films grown on Si/SiO_2 substrates are performed using x-ray diffraction and AFM imaging. The x-ray diffraction pattern shown in Fig. 6(a), indicates that the as deposited F_4CuPc thin-film on Si/SiO_2 is highly ordered with a diffraction peak at 6.55° (2Θ) corresponding to a d-spacing of 1.35 nm. The observed d-spacing for F_4CuPc thin film is similar to that for CuPc (1.29 nm) and F_{16}CuPc (1.42 nm), which indicates that all of these CuPc derivatives have similar crystal structure as expected from their similar molecular structure and relatively small size of the fluorine atom.[14] AFM image of F_4CuPc thin-films on Si/SiO_2 substrates show the arrangement of randomly oriented grains of various sizes in the range of 100–200 nm and it supports polycrystalline nature of F_4CuPc thin film, as shown in Fig. 6(b).

In partially ordered organic semiconductors, such as the materials employed in this study, charge transport occurs by hopping of charge carriers in a manifold of localized states. The profile of the electronic density of states has been suggested to be Gaussian[15,16] or Exponential.[17,18] The creation of additional deep trap states will result in a reduction of mobility. The *n*-channel field effect transistor (FET) forming materials with a LUMO level close to vacuum are particularly susceptible to electron trapping because the traps produced by oxygen and moisture lie at a lower energy compared to normal transport states of such materials. This can result in a significant lowering of electron transport mobility, which occurs in many materials. The use of appropriate dielectrics, with a low concentration of electron traps, will permit *n*-channel operation in an inert environment. However,

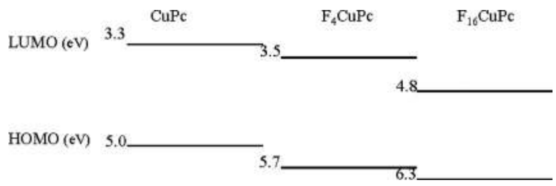

FIG. 7. LUMO and HOMO energy levels scheme of CuPc, F_4CuPc, and F_{16}CuPc molecules.

as this work clearly shows, exposure to air will destroy electron transport unless the LUMO energy is sufficiently away from vacuum to be relatively unaffected by traps resulting from exposure to moisture/oxygen and also other atmospheric constituents. This is the reason why F_{16}CuPc and PDI-8CN_2 are such good *n*-channel FET forming materials. Given the importance to stability for practical applications involving printing processes, we propose that the LUMO level must remain a key criterion in the selection of materials for *n*-channel organic FETs. Thus, while the modification of the dielectric interface (by the use of materials such as PMMA) does permit electron transport in inert environments, this does not guarantee similar behavior when exposure to ambient conditions occurs.

The LUMO and HOMO energy levels for CuPc and fluorinated CuPc are shown in Fig. 7. In the family of PCs, CuPc mainly transports holes in TFTs with a HOMO level of 5.0 eV and the LUMO level 3.3 eV below vacuum.[19] The LUMO level is too close to vacuum to effectively compete with trap states for electrons in structures involving most gate insulators. Thus, induced electrons are immobile in CuPc. On the other hand, in F_{16}CuPc, the LUMO level (4.8 eV) as well as the HOMO level (6.3 eV) is lowered by more than 1 eV with respect to CuPc.[20] When the LUMO states are able to compete with trap states for the induced electrons, either by adjusting the LUMO levels of semiconductors or by changing the trap profile through gate dielectric modification, this leads to the *n*-channel behavior in air by many groups.[3,21] The partial fluorination (F_4CuPc) presents a very interesting intermediate case with LUMO and HOMO levels of 3.5 and 5.7 eV, respectively, and important to study the effects of energy level tuning on charge transport.[22] In this work, we have shown that the partial fluorination of CuPc results in a lowering of LUMO and HOMO energy levels, which leads a transformation of TFT transport as described below.

In F_4CuPc devices with a SiO_2 gate dielectric, hole transport dominates over electron transport, whereas in devices with PMMA/SiO_2 bilayer dielectric in which the PMMA is immediately adjacent to the semiconductor, electron transport is enhanced. Both types of devices exhibit ambipolar transport to some degree. While in case of CuPc devices, weak electron transport is observed in addition to dominant hole transport with PMMA/SiO_2 dielectrics. Obviously, the SiO_2/PMMA dielectric enhances electron transport in both materials but enhancement is enhanced in the case of F_4CuPc due to the lowering of LUMO as compared to CuPc.

Once the devices are exposed to air/moisture, a high concentration of electron traps are generated in the organic thin film semiconductors, suppressing electron transport in the corresponding devices. In the case of F_4CuPc OTFTs with PMMA/SiO_2, electron transport is significantly recovered after annealing of the devices inside the glove box at 100 °C which confirms the presence of air/moisture induced traps in devices and their deleterious effects on electron transport. The recovery of electron transport (under nitrogen) in the case of F_4CuPc devices is mainly due to its low LUMO level as compared to LUMO of CuPc. On the other hand F_{16}CuPc devices have not shown any significant degradation in electron transport upon exposure to air, which is a consequence of their high electron affinity.

IV. CONCLUSIONS

Our study demonstrates that in general, it is the energy levels that fundamentally determine how efficiently each carrier type moves in OTFTs. The choice of gate insulator can in some cases change the trap depth distribution sufficiently so as to radically alter the nature of transport. Our results with PMMA do demonstrate this effect to some degree as well. But such changes in the nature of charge transport are limited to inert ambient. Once devices are exposed to air/moisture, the electron trap density increases and results in the significant suppression of electron transport in organic molecules.

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