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Structural and electrical properties of silicon dioxide layers with embedded germanium nanocrystals grown by molecular beam epitaxy

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A sheet of spherical, well-separated, crystalline Ge nanodots embedded in SiO_2 on top of a p-(001)Si wafer was fabricated by molecular beam epitaxy (MBE) combined with rapid thermal processing and characterized structurally and electrically. The average size of the Ge nanodots was estimated to be 4.5 nm with an average aerial density of 3×10^{11} cm^{-2}, situated at 4.4 nm in average away from the Si/SiO_2 interface. Significant charge storage effects were observed through capacitance–voltage measurements of metal–oxide–semiconductor capacitors. © *2003 American Institute of Physics.* [DOI: 10.1063/1.1555709]

Recently, considerable attention has been focused on semiconductor nanoparticles embedded into the silicon dioxide (SiO_2) of a metal–insulator–semiconductor (MOS) device for future high speed and low power consuming logic and memory devices.[1,2] The use of a floating gate composed of isolated dots reduces the problems of charge loss encountered in conventional Flash memories, allowing for thinner injection oxides and, hence, smaller operating voltages, better endurance, and faster write/erase speeds.[1,3] Moreover, the performance and the success of such a memory structure strongly depend on (a) the process ability for making uniform and reproducible thin tunnel oxides and (b) the characteristics of the islands (such as crystallinity, size, shape, orientation, spatial distribution) that influence both the potential energy of trapped electrons and the Coulomb blockade energy, which prevent the injection and storage of more electrons.[3] Self-assembling of silicon (Si) or germanium (Ge) nanocrystals (ncs) in SiO_2 layers has been studied by a large number of groups[1–4] and strong memory effects in MOS devices using such oxides were reported.[1–5] Nanocrystals have been fabricated using low-energy-ion implantation[6,7] and different deposition techniques.[2,8,9] In this letter, we demonstrate a growth technique, which is capable of meeting the earlier requirements; the method is based on molecular beam epitaxy (MBE) combined with rapid thermal processing (RTP).

Prior to MBE deposition, uniform and pure SiO_2 buffer layers of thickness 4 and 7 nm were grown on chemically cleaned 4 in. p-type (001) Si wafers of resistivity 1.8–2.2 Ωcm in an oxygen (O_2) ambiance. A $\sim$1-nm-thick SiO_2 layer was removed from the top surface *in situ* using a Si flux of 0.035 nm/s at 850 °C before Ge deposition in a Semicon VG80 MBE system as described in detail elsewhere.[10] A Ge layer of thickness 0.7 nm was then grown on the 4- and 7-nm-thick SiO_2 covered Si wafers, named as wafer 1 and 2, respectively, with a rate of 0.02 nm/s at 350 °C; this was followed by the deposition of a capping layer of polycrystalline Si of thickness 4 nm, with a rate of 0.05 nm/s at the same temperature. A reference sample without the Ge layer was prepared on a 4-nm-thick SiO_2 covered Si wafer (wafer 3). The sandwiched Si/Ge/SiO_2/Si samples were heat treated by RTP in an O_2 ambiance at 800 °C between 10 and 20 min. A substantial amount of germanium oxide (GeO_2) clusters was formed during this oxidation step.[5,11] Transformation of the GeO_2 clusters into Ge–ncs (called reduction) was done by thermal treatment at 950 °C in a N_2 atmosphere between 5 and 40 s. The structure of the samples was characterized by transmission electron microscopy (TEM) of plan-view and cross-sectional geometries with a Philips CM20 instrument operating at 200 keV and a few samples were investigated by high resolution TEM (HRTEM). The composition and structure of the samples were controlled by Rutherford backscattering spectroscopy (RBS)/channeling using a 1.5 MeV He^+ beam.

Prior to high frequency capacitance–voltage (C–V) measurements of wafers 1 and 2, aluminum (Al) gate capacitors were fabricated by performing chemical cleaning followed by annealing at 800 °C for 10 min in N_2, backside oxide removal, Al deposition, and patterning and sintering processes. Another set of capacitors were fabricated for C–V measurements after deposition of 15-nm-thick SiO_2 by the low-pressure chemical vapor deposition/tetraethoxysilane method in addition to the earlier processes to suppress leakage current.[1]

The oxidation and reduction conditions were optimized with respect to negligible Ge segregation at the Si/SiO_2 interface, uniform dot-size distribution around 4 nm, a tunnel-oxide thickness of about 4 nm, a dot density $\leqslant 10^{12}$ cm^{-2} (electron transport between the dots was observed for a dot density larger than 10^{12} cm^{-2}), and the largest possible charge storage capability. These conditions were found to be 14 min oxidation at 800 °C in O_2 followed by 30 s annealing

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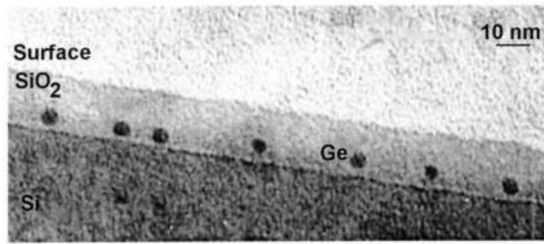

FIG. 1. Bright-field image of a cross-section sample from wafer 1, oxidized at 800 °C for 14 min in O_2 followed by reduction at 950 °C for 30 s in N_2. Ge–ncs show a dark contrast on the gray background of the SiO_2 layer.

at 950 °C in N_2. The samples discussed in the following are all processed under these conditions.

Figure 1 represents a typical bright-field, cross-section TEM (XTEM) image taken with the electron beam direction close to the (110)-zone axis in strongly underfocused condition of a sample from wafer 1. Under this condition, the Ge–ncs show a dark contrast on a gray background. Spherical and well-separated Ge–ncs embedded in the SiO_2 layer are clearly observed. The average distance of the dots from the Si substrate is measured to be 4.4 nm [Fig. 2(a)] and the average distance between the dots can be directly measured on such XTEM images. The mean size and density of the dots are measured under the same imaging conditions but on plan view specimens. Typical values of size and aerial density are found to be 4.5 nm and 3×10^{11} cm^{-2}, respectively,

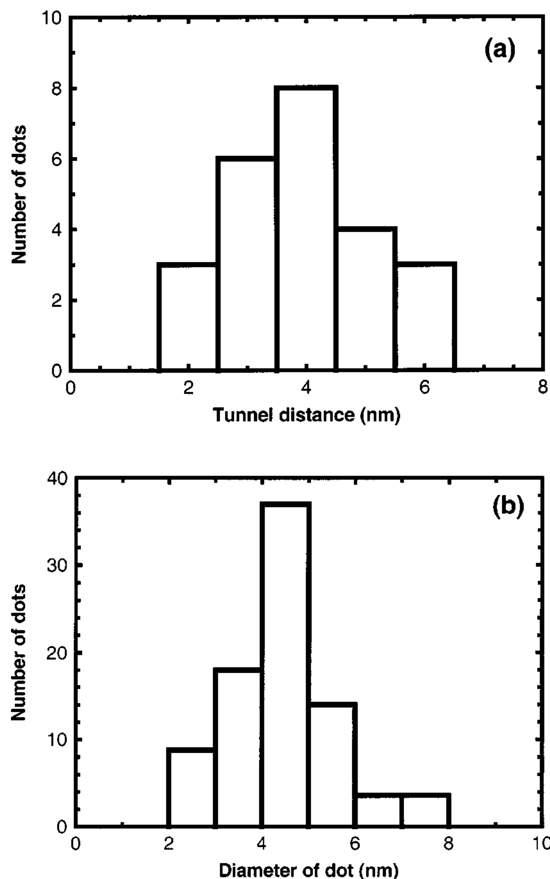

FIG. 2. Distributions of tunnel injection distance, i.e., the distance between a Ge nanocrystal and the Si substrate (a) and size of the Ge–ncs (b), for sample of wafer 1, oxidized at 800 °C for 14 min in O_2 followed by reduction at 950 °C for 30 s in N_2. The mean values ± the standard deviations of these distributions are (4.4±1.4) and (4.5±1.8) nm, respectively.

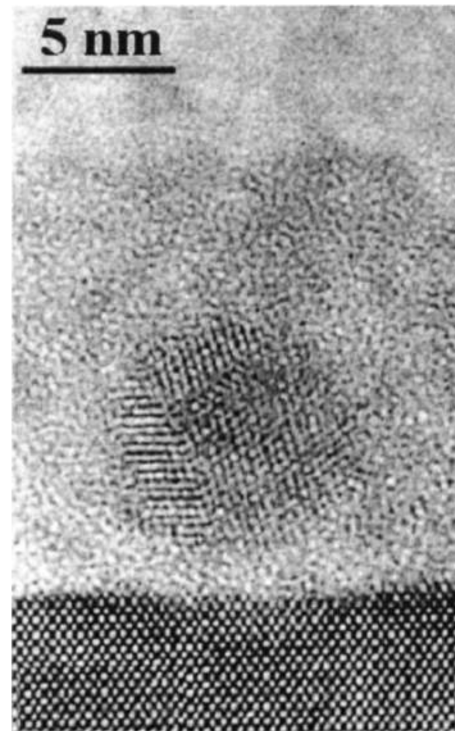

FIG. 3. HRTEM image of a crystalline isolated Ge nanodot.

on wafer 1 [Fig. 2(b)]. Moreover, the crystalline nature of the Ge dots is evidenced in HRTEM images such as the one shown in Fig. 3. In such large dots (~7 nm) twinning of the {111} planes is observed while the distance from the dot to the substrate could be as small as 2 nm. The results are also found to be similar for samples from wafer 2.

The RBS/channeling results elucidate the recovery of Ge from its oxide state during reduction without Ge diffusion (not shown). A strong evidence of charge storage effect in the crystalline Ge-nanodot layer is demonstrated by the anticlockwise hysteresis behavior in the high-frequency $C-V$ characteristic for a sample from wafer 1 (Fig. 4). High positive and negative gate voltages cause the $C-V$ curves to shift in the direction of stored negative and positive charges, respectively, while no hysteresis appears at 2 V gate voltage

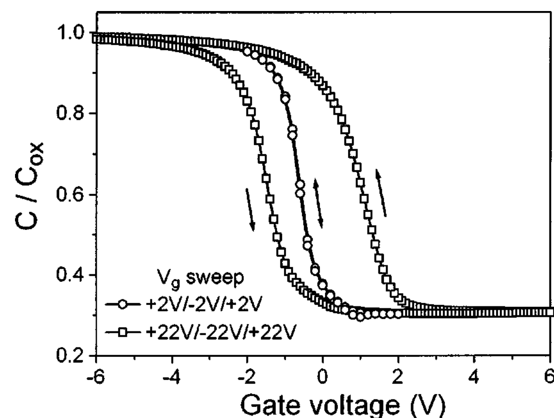

FIG. 4. High-frequency $C-V$ curves of samples from wafer 1, oxidized at 800 °C for 14 min in O_2 followed by reduction at 950 °C for 30 s in N_2. High positive and negative gate voltages cause electron and hole injections respectively into the oxide from the substrate. A gate voltage (V_g) sweep from inversion to accumulation and from accumulation to inversion is shown by the arrow to the left and to the right, respectively.

(V_g) sweep. In the former case, charge trapping occurs through electron and hole injection from the substrate into the oxide. A gradual increase in the flatband voltage shift (ΔV_T) with increasing V_g sweep until 22 V is also observed and ΔV_T is measured to be 0.5 V for $V_g = 6$ V. No flatband voltage shift is observed for the reference sample prepared from wafer 3 by oxidizing only at 800 °C for 14 min in O_2 ambiance, implying that the memory effect is Ge nanocrystals related. A similar flatband voltage shift is also observed for samples from wafer 2.

The self-assembling phenomenon of Ge nanodots in SiO_2 can be explained using the Ostwald ripening mechanism,[12] which describes the growth of larger particles at the expense of smaller particles. Shklyaev *et al.*[13] showed that thin MBE grown Ge layers on a Si substrate covered with a thin SiO_2, formed a high density of hemispherical Ge island with some connected islands. Such a structure could initiate the Ostwald ripening mechanism as it requires diffusion of Ge atoms from the peripheral/valley regions of Ge islands towards their respective centers to construct spherical dots for achieving greater volume to surface ratio. In our case, TEM investigations demonstrate that all the islands are connected until the oxidation of the Si capping layer is completed. Thus, the Ge-dot formation takes place after complete oxidation of the Si capping layer but still during the oxidation process. An appreciable amount of Ge is oxidized during the Ge-dot formation.[5,11] For this reason the reduction process is essential to recover the Ge nanodots from their oxide state. During thermal treatment in a N_2 ambiance, the GeO_2 clusters are reduced by Si atoms arriving from the SiO_2/Si interface according to the chemical reaction $Si + GeO_2 \rightarrow Ge + SiO_2$.[14] It is revealed from Fig. 1 that the Ge dots are formed near to their initial positions, which could be due to a smaller Ge diffusion coefficient compared to Si.[14] A reduction time longer than the optimized one leads to the formation of bigger Ge–ncs by coalescence of smaller Ge–ncs and a concomitant reduction in the tunneling distance. Thin Ge layer produces small dots and the homogeneity of the dot size is also correlated with the uniformity of the thickness of the Ge layer. The advantage of using MBE for the deposition of the Ge and Si layers is the precision by which very thin (e.g., 0.7 nm) uniform layers can be deposited.

In summary, we have demonstrated a fabrication technique, which is capable of producing a layer of crystalline Ge nanodots in SiO_2, based on MBE in conjunction with optimized RTP. The Si/Ge sandwiched layers were grown by MBE on 4- and 7-nm-thick SiO_2 covered p-Si wafers. The structural investigations were performed by TEM, HRTEM, and RBS/channeling. The average dimension of the Ge–ncs were found to be 4.5 nm with average aerial density of 3×10^{11} cm^{-2}. The average tunneling oxide thickness was estimated to be 4.4 nm. Twins were observed in some bigger crystalline dots of ~7 nm. Finally, a significant memory effect was manifested by the hysteresis in the high-frequency $C-V$ measurements for the optimized samples.

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