Mechanisms leading to erratic snapback behavior in bipolar junction transistors with base emitter shorted

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Mechanisms leading to erratic snapback behavior in bipolar junction transistors with base emitter shorted

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This paper discusses two different modes of breakdown in the reverse-biased *I–V* characteristics observed generically in bipolar junction transistors (BJTs) with the base emitter shorted, showing an erratic behavior, in the presence of large displacement currents. Experimental observations related to reverse-biased collector junctions of BJTs, that exhibit two different states of breakdown when a fast voltage ramp is applied are presented. Numerical simulations of the transient behavior of avalanche injection in $p/n^-/n^+$ structures show that two very close breakdown states coexist. The mechanisms leading to the erratic behavior of the second breakdown are discussed. The jittery nature of the breakdown is attributed to the delay associated with the buildup of the electric field across the n^-/n^+ junction. © *2005 American Institute of Physics*. [DOI: 10.1063/1.1874294]

I. INTRODUCTION

Displacement current has been shown to play an important role in the fast switching behavior of the matrix of transistors in the Marx bank circuit shown in Fig. 1. In this circuit, the voltage across each of the reverse-biased p/n junctions collapses due to the application of a fast voltage ramp.[1] Transistorized Marx bank circuits are used for generating high voltage, fast rising pulses for driving pockel cells used for optical pulse switch out in ultrashort-pulse lasers. It has been observed that when the reverse bias across a p/n junction increases sharply near the breakdown region, producing a large displacement current, the device may exhibit either of two different types of breakdown.[1]

The sudden collapse of voltage across the p/n junctions and bipolar junction transistors, called second breakdown (SB), is always preceded by an increased current due to an avalanche breakdown and a delay time before the initiation of the breakdown.[2–14] Typically, shorter delays of a few nanoseconds occur for current-mode second breakdown,[8,15–19] while larger delays of milliseconds have been attributed to thermal initiation.[4–7] For both of these triggering mechanisms, second breakdown is believed to be due to the positive feedback nature of the current-controlled negative resistance, causing the constriction of current through narrow conducting regions known as hot filaments. In thermal-mode breakdown, the negative resistance is due to enhanced carrier generation caused by heating effects from the generated carriers, while in current mode the effect is due to the avalanche injection at the n^-/n^+ junction. The negative resistance due to transit-time effects in $p-\nu-n$ structures has been extensively studied and has many applications in microwave devices.[21–25] However, under steady-state conditions at high breakdown current densities in $p-\nu-n$ structures, current-mode second breakdown has been, observed and attributed due to the avalanche injection from both the p/n^- and n^-/n^+ junctions.[5] A related behavior- avalanche injection phenomena in bulk silicon $n^+/n^-/n^+$ devices have also been observed at high current levels and explained due to the saturation of the carrier drift velocity at high electric fields and charge storage in the neutral region that causes the electric field to peak at the n^-/n^+ junction.[5–8] In BJTs with an $n^+/p/n^-/n^+$ structure, high current densities occur during turn-on and turn-off transients when lateral flow of base current produces a voltage drop across the emitter-base junction that leads to the base push-out effect, also known as "current-induced avalanche injection."[8,14,17–20] In the absence of base drive, fast switching has also been observed in BJTs in a class of devices called "avalanche transistors," in which

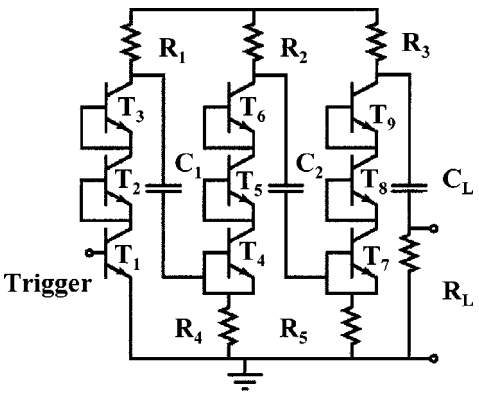

FIG. 1. Schematic figure showing Marx bank circuit.

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current injection from the emitter-base junction results in redistribution of the electric field across the collector region.[17–20] It has been experimentally[1] shown that when a fast pulse is applied across the BJT with the base and emitter shorted, the device unpredictably exhibits one of the two modes of breakdown, which is termed erratic mode second breakdown (EMSB) in the rest of this paper.[1] In another related breakdown mode, trapped plasma avalanche transit time (TRAPATT) mode of operation, collapse of voltage across reverse-biased $p-n$ junction and its dependence on displacement current has been attributed due to "shock-wave-like" avalanche breakdown electric field, traversing the entire junction.[20–25] In this mode of operation, the role of avalanche injection across n^+/n^- junction is not considered during the snapback. We investigate the role of propagation of the avalanche shock wave and the collapse due to the avalanche injection at n^+/n^- in this work. Understanding the physics of breakdown will be of utmost importance to generation of fast and short electrical pulses, which have an important application among others in reliability testing of electrostatic discharge (ESD) protection in complementary metal-oxide semiconductor (CMOS) circuit.[13]

We describe the generic nature of the erratic and non-catastrophic behavior of the second breakdown found in $n-p-n$ transistors having lowly doped collector regions. This work demonstrates a one-dimensional (1D) numerical simulation method to understand the physical mechanisms involved in EMSB in $p/n^-/n^+$ structures. We have associated the process of double injection in TRAPATT breakdown mode to explain the erratic behavior in device breakdown. Through transient simulations, injection across the n^-/n^+ junction due to the buildup of current resulting from avalanche breakdown at the p/n^- junction is demonstrated and two distinct modes of breakdown are shown.

The experimental results related to application of fast pulses across the reverse-biased junctions are discussed in Sec. II. Section III presents the physics behind the interaction of avalanche-generated carriers with the field in $p/n^-/n^+$ silicon structures and the subsequent avalanche injection at the n^-/n^+ junction, leading to snapback across the junction. In this work we have simulated an otherwise complex three-dimensional (3D) behavior of transient simulation of the dynamics of avalanche breakdown by relating it in 1D simulation with the role of enhanced current conditions at the electrode during the transient process. Numerical simulations demonstrating the avalanche injection mechanism and snapback are presented in this section and an explanation of the erratic characteristics of the breakdown is proposed.

II. EXPERIMENTAL OBSERVATIONS AND DISCUSSION

A. Application of high voltage ramp in BJTs with Base Emitter Junction Shorted

In earlier experimental work,[1] the application of fast rise-time, high voltage pulses across a reverse-biased $p-n$ junction of an $n-p-n$ transistor (Motorola 2N5551) with the base and emitter shorted was observed to cause an erratic collapse of the voltage. The experiment was repeated with

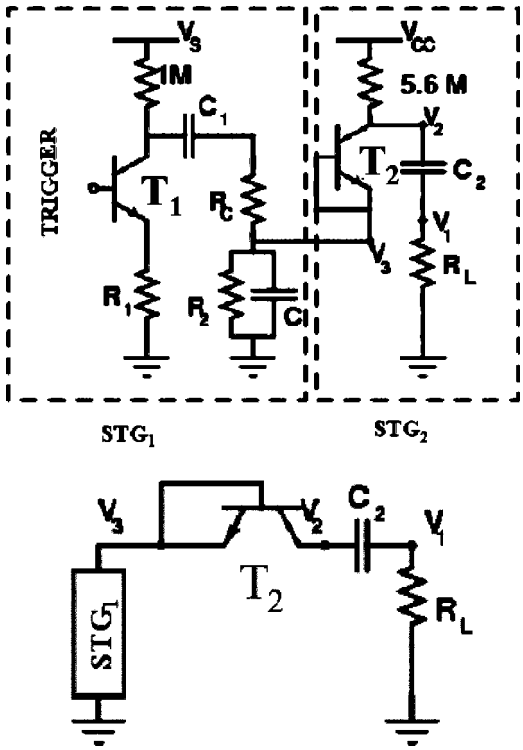

FIG. 2. Circuit for application of high voltage pulses across the reverse-biased $p-n$ junction. Stage 1-produces a negative outgoing pulse and resultings in a pulse across device under test (T_2).

$n-p-n$ devices (2N5551, 2N5550, 2N2222A, and 2N2221) from different manufacturers and different lots.

The experimental circuit used for applying high voltage pulses across the reverse-biased junction of the device under test (transistor T2) is shown in Fig. 2. The experimental circuit comprises two stages; the first stage produces a negative pulse as the capacitor C_1 discharges. The negative-going pulse causes the voltage to rise across the device under test.[1] Changing the values of resistance R_C and capacitance C can adjust the ramp speed of the first stage pulse appearing across the junction. The device under test can be biased to different voltages by changing V_{CC}. Thus changing the bias voltage V_{CC} can vary the prebreakdown current across T2 prior to the application of the pulse.[1]

In Fig. 3, the bias voltage is first set at $V_{CC}=300$ V (with reference to Fig. 2), when the negative-going first stage pulse causes a reverse biasing pulse to appear across the collector-base junction[1] of T2. After an initial rise of voltage across the device (A^1 B^1), during which the current across the junction is a displacement current, the same device exhibits two different modes of breakdown ($B_1{}^1$ in curve "1*s*" or $B_2{}^1$ in curve "1*p*"). The device either goes to the avalanche breakdown mode or to the secondary breakdown mode. In the avalanche mode, the current continues to increase and the voltage remains clamped to the breakdown voltage. However, in the second breakdown mode, the voltage collapses and the transistor remains clamped in a low voltage and high current state. As the rise time of the input pulse decreases, the device shows greater preference for the SB mode. For extremely fast pulses (rise time <10 ns) the device always exhibits the second breakdown behavior. Similarly, for lower

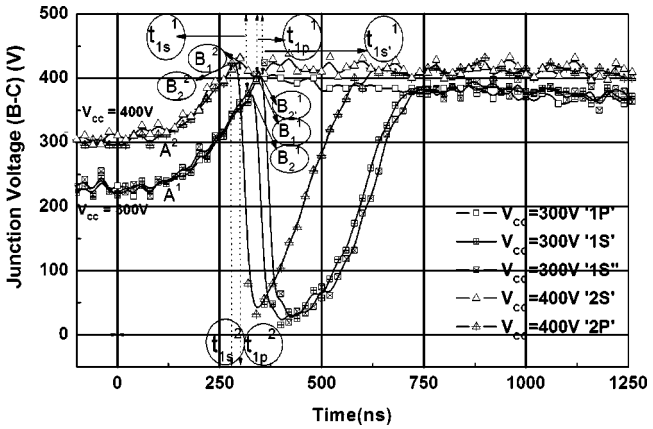

FIG. 3. Base-collector junction voltage vs time for a Motorola 2N5551 biased to different voltages prior to the application of the voltage pulse. Prebiasing to different voltages leads to a flow of breakdown current prior to application of the stage 1 pulse. Circuit elements (with reference to Fig. 2) are R_C=662 Ω, C =470 pF, C_1=C_2=1 nF, R_1=56 Ω, R_2=158 kΩ, and R_L=11 kΩ. Supply voltage V_S=350 V and V_{CC} =300 V.

ramp speeds (rise time >500 ns) the device only exhibits an avalanche mode breakdown. The bias voltage is set at V_{CC} =400 V across the device, such that a breakdown current flows across the junction of T2 for a considerable time (over 10 min) after which fast pulses are applied. In each of the cases, the device under test shows a similar rise of voltage each time the fast pulse is applied from the first stage (A^2 B^2). The device goes unpredictably to the two different states of breakdown ($B_1{}^2$ in curve "2*s*" or $B_2{}^2$ in curve "2*p*"). After going into the state, the device recovers to the same voltage that appears across the device in the avalanche mode of breakdown.

The breakdown point B is marked by the two possible states of breakdown and the delay between the trigger pulse and the transition point B [shown as ($t^1{}_{1p}$, $t^1{}_{1s}$, $t^1{}_{1s'}$) and ($t^2{}_{1p,}$ $t^2{}_{1s}$) in Fig. 3] exhibits jitter for voltage ramps having similar speed. The jitter for a given ramp speed is defined as the variation in the maximum and minimum delays between the 90% point of the trigger pulse and the transition point B (measured on a digital storage oscilloscope using the infinite persistence mode of operation). The jitter decreases sharply as the ramp speed is increased. For a Motorola 2N5551-transistor and a voltage ramp having a fall time of 100 ns, the jitter is approximately 10 ns and this decreases to 200 ps for a ramp with a fall time of 1 ns. However, for a particular ramp speed, the breakdown voltage associated with second breakdown at $B^1{}_2$ is less than the primary voltage at $B^1{}_1$, which is however higher than another second breakdown event at $B^1{}_2$ illustrating that the nature of breakdown is erratic.

The above experiments were repeated with different devices (2N5551, 2N5550, 2N2222A, and 2N2221) from different manufacturers and different lots, but other than the value of the breakdown voltage, the erratic behavior of the breakdown was found to be generic in all devices. Figure 4 shows the jittery nature of breakdown for a 2N2221 device having lower breakdown voltage (BV_{CBO}=60 V). These low breakdown-voltage devices, though exhibiting this erratic behavior, have a much sharper transition region. The transition between the two modes of breakdown in these devices caused by a change in the ramp speed is very abrupt.

To summarize the features of the breakdown,

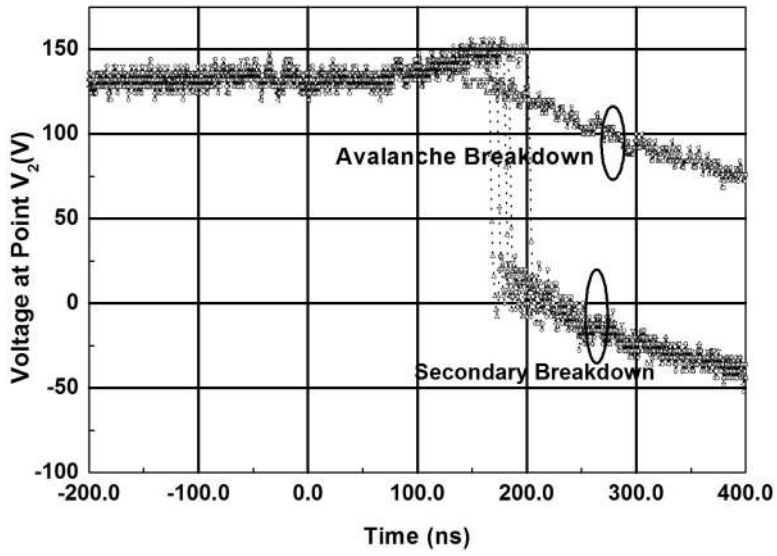

FIG. 4. The voltage measured at node V_2 (with reference to Fig. 2) when device under test (DUT) is 2N2221(Motorola). The erratic-mode SB observed in 2N2221 devices has lower breakdown voltage.

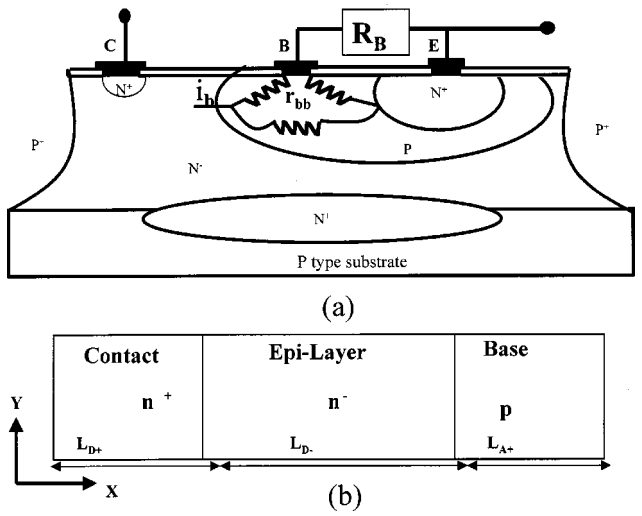

FIG. 5. Cross section of an $n-p-n$ transistor. In the experiment the base and emitter were shorted and the region of interest is the $p/n^-/n^+$ structure used for simulation purpose shown in (b). Ramped voltages were applied across the structure.

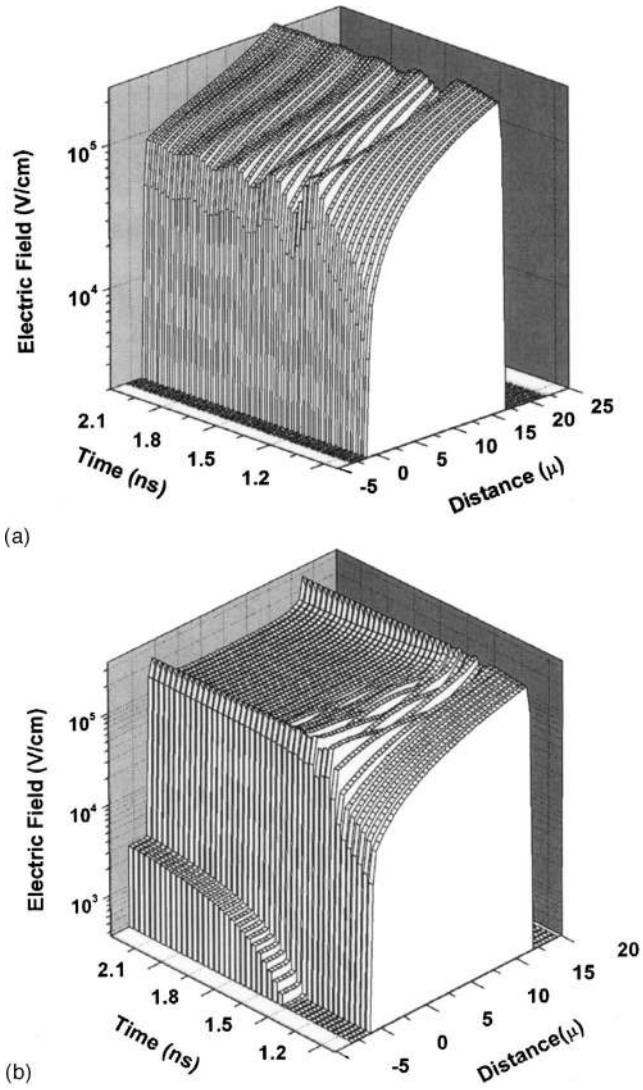

FIG. 6. (a) Electric-field distribution in a $p/n^-/n^+$ structure ($N_D^+ = 10^{18}/\text{cm}^3$, $N_D^- = 10^{15}/\text{cm}^3$, and $N_A^+ = 10^{19}/\text{cm}^3$; $L_{A+} = 5\ \mu$m, $N_D \sim 10^{15}$, $L_{D-} = 18\ \mu$m, and $L_{D+} = 2\ \mu$m) (with reference to Fig. 5) for load resistance $R_L = 10\ \text{M}\Omega$ when a voltage is ramped to 350 V in 1.5 ns. No avalanche injection is initiated at the n^-/n^+ junction. (b) Electric-field distribution in a $p/n^-/n^+$ structure structure ($N_D^+ = 10^{18}/\text{cm}^3$, $N_D^- = 10^{15}/\text{cm}^3$, and $N_A^+ = 10^{19}/\text{cm}^3$; $L_{A+} = 5\ \mu$m, $N_D \sim 10^{15}$, $L_{D-} = 18\ \mu$m, and $L_{D+} = 2\ \mu$m) for load resistance $R_L = 100\ \text{k}\Omega$ when a voltage is ramped to 350 V in 1.5 ns (with reference to Fig. 5). Avalanche injection is initiated at the n^-/n^+ junction leads to a sharp snapback effect.

(1) There are two distinct types of breakdown.
(2) In the second breakdown mode, the device undergoes a large drop in the voltage of about 200 V.
(3) In the normal avalanche mode, the device shows a slight negative resistance with drop in voltage of about 25 V.
(4) Under similar excitations, the device may choose either of the two modes of breakdown.
(5) The rate at which the voltage ramp is applied has an impact on the breakdown characteristics. With faster ramp speeds, the device preferably goes to the second breakdown state but with slower ramp speeds, the device is more likely to go into the normal avalanche mode breakdown. The delay between the trigger pulse and the point when the breakdown occurs is of the order of nanoseconds.
(6) Both modes of breakdown are observed in devices with different breakdown voltages.
(7) Application of the fast rising pulse across the base-collector terminal of the transistor with the emitter terminal left open led to catastrophic failure of the device.

B. Similarity with TRAPATT Operation

The device behavior is analogous to TRAPATT operation, in which the application of a voltage pulse across a Si $p-n$ junction with sufficient time rate of change (dV/dt) can produce an electron-hole plasma that causes the breakdown electric field to fall significantly, trapping the plasma.[21–25] Such an ionization wave front is typical of $p/n^-/n^+$ structures, where the n^- region is very lightly doped to the order of $N_D \sim 10^{14}\ \text{cm}^{-3}$ and the time of the propagation are of the order of a few hundreds of picoseconds. In our experiments, the erratic choice between the two breakdown modes exists for ramp rates ranging from 0.002 to 0.02 KV/ns—magnitude of the ramp rate changes an order of magnitude and the device still exhibits the unpredictable nature of breakdown. Changes in the critical breakdown field due to temperature variation can be ruled out, as the device shows no change in the characteristics when a large current flows through the device before the measurement, heating it up.

The behavior of snapback and its subsequent recovery has been experimentally demonstrated to be generic in BJTs having breakdown voltages (BV_{CBO}) ranging from 60 to 80 V. In the experiment, the emitter-base junction was shorted and the base-collector portion of the device looks like the $p/n^-/n^+$ structure shown in Fig. 5. To confirm that the emitter-base junction is not "turned-on" when the pulse was applied across the transistor, resistors of variable value were placed between the emitter and base terminals of the device under test (T2) and the above experiments were repeated. For relatively low values of resistance ($R_B = 47\ \Omega$), the voltage

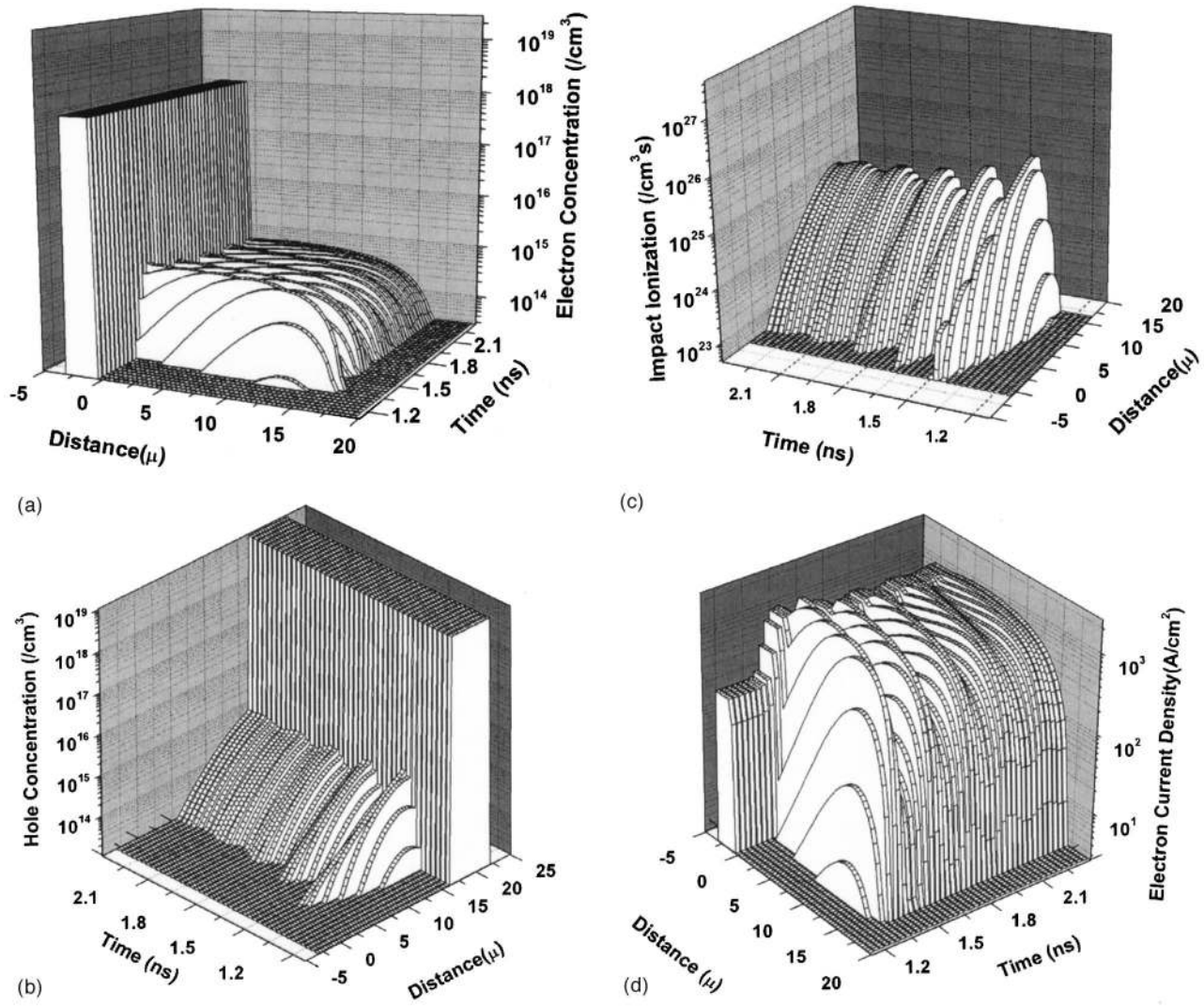

FIG. 7. Profiles of (a) electron concentration, (b) hole concentration, (c) impact generation, and (d) electron current density when the voltage is ramped to a final voltage of 350 V in 1.55 ns across a device having a $p/n^-/n^+$ structure ($N_D^+=10^{18}/\text{cm}^3$, $N_D^-=10^{15}/\text{cm}^3$, and $N_A^+=10^{19}/\text{cm}^3$; $L_{A+}=5$ μm, $N_D\sim 10^{15}$, $L_{D-}=18$ μm, and $L_{D+}=2$ μm) (with reference to Fig. 5) and the load resistance $R_L=10$ MΩ. Under these conditions current-induced avalanche injection does not lead to regenerative second breakdown process.

across the device increased in the same way described above. However, for relatively large resistance values ($R_B=452$ kΩ), the voltage across the device was clamped at 218 V, with no increase in voltage across the device. It may be possible that the emitter-base junction may be conducting in subthreshold region resulting from voltage drop due to lateral flow of current through the base when the emitter base is shorted. However, it was observed that flow of breakdown current prior to the application of pulse which would have further turned on the emitter-base diode, does not alter the erratic behavior. These experimental results show that the unpredictable breakdown behavior is not related to crowding of current injected from the base to emitter, which is one mechanism that can initiate second breakdown.[9,26,27] We propose a mechanism to explain the erratic choice of breakdown modes based on the phenomenon of avalanche injection in an $n^+/p/n^-/n^+$ structure in the next section.

III. MECHANISMS

A. Simulation and Model

In TRAPATT mode large displacement current has been shown to cause propagation of shock wavelike pattern in the electric field across the reverse-biased junction. Role of increased current densities leading to a double avalanche injection mechanism has not been considered during the propagation of the above phenomenon. Steady-state breakdown current results when transients involving the propagation of shock wave phenomenon had settled down for a given breakdown voltage across the device and high level of current densities under steady-state conditions causes double injection mechanisms in $p/n^-/n^+$ structures. In this section we associate the two mechanisms to understand the erratic behavior of the device. The role of displacement current in the 3D structure has been incorporated through 1D transient

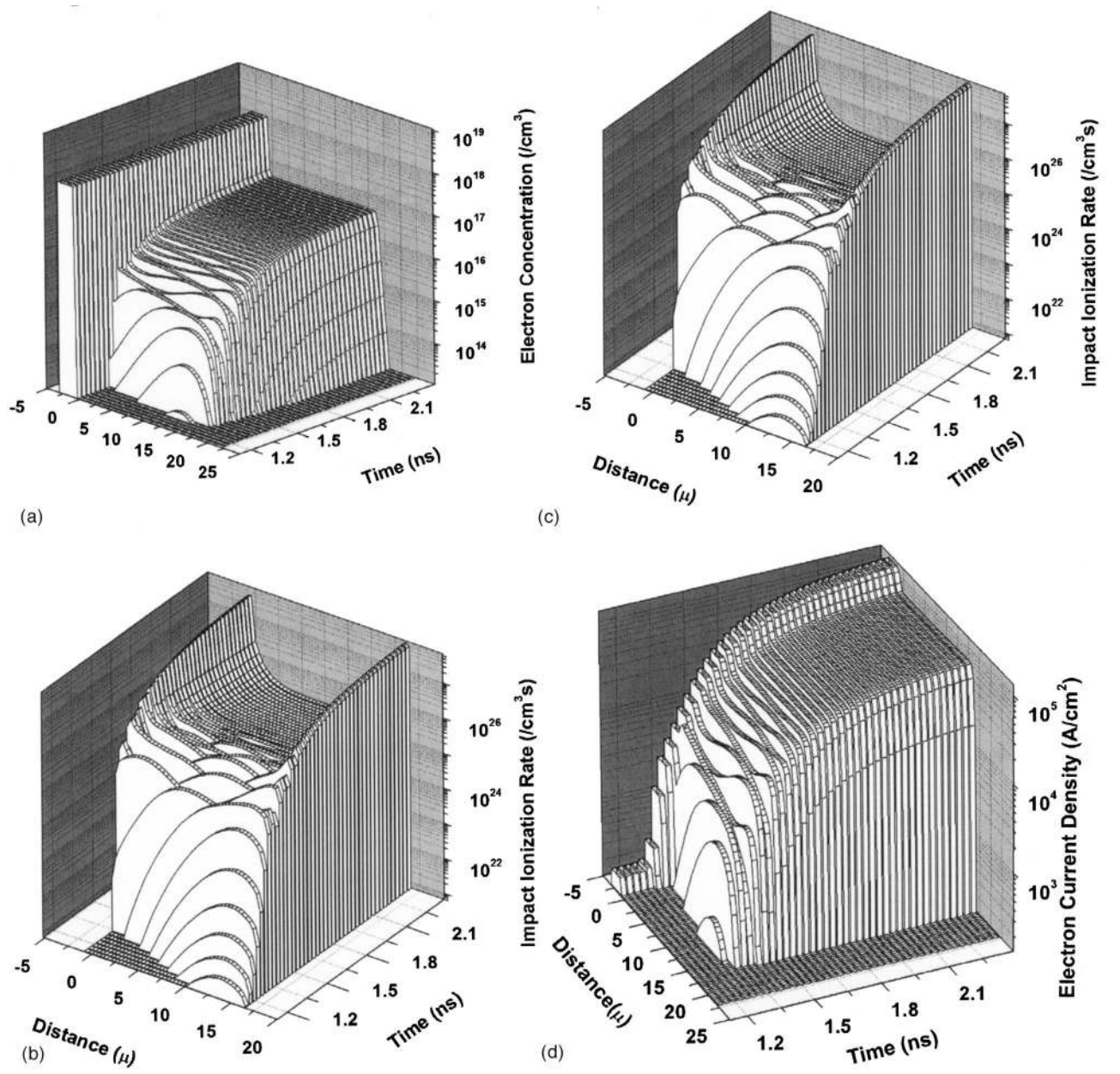

FIG. 8. Profiles of (a) electron concentration, (b) hole concentration, (c) impact generation, and (d) electron current density when the voltage is ramped to a final voltage of 350 V in 1.55 ns across a device having a $p/n^-/n^+$ structure ($N_D^+=10^{18}/\text{cm}^3$, $N_D^-=10^{15}/\text{cm}^3$, and $N_A^+=10^{19}/\text{cm}^3$; $L_{A+}=5$ μm, $N_D\sim10^{15}$, $L_{D-}=18$ μm, and $L_{D+}=2$ μm) (with reference to Fig. 5) and the load resistance $R_L=100$ kΩ. Under these conditions current-induced avalanche injection takes place across the n^-/n^+ junction, resulting in second breakdown.

simulation using variable load resistors, which accounts for the role of increased current density for faster ramps.

This section presents simulation results pertaining to current-induced avalanche injection in $p/n^-/n^+$ structures during the propagation of shock wave across the junction. The device simulations were performed using the two-dimensional (2D)-device simulator ATLAS.[28] The impact-ionization model used for the simulation was the Selberherr model[28] and a $p/n^-/n^+$ diode structure with varying junction length and varying external load was used for the simulations.

The buildup of the electric-field profile is shown in Fig. 6(a) when the voltage is ramped to 350 V in 1.5 ns with a load resistance of $R_L=10$ MΩ. Avalanche breakdown is initiated in the p/n^- junction depletion region as the voltage reaches 290 V in 1350 ps [the electric field at the n^-/p^+ is 2.9×10^5 (V/cm) and impact generation rate is 5×10^{22} (/cm^3 s)]. The ionization wave front travels like a shock wave that propagates through the n^- region from time $t_s=1350$ ps to $t_s=1460$ ps. After the initiation of the avalanche process, the generated carriers move from the p/n^- junction to the n^- region. The generated carriers modulate the electric field to peak at the n^-/n^+ junction and the field distribution changes its profile from triangular shape with one peak at p^+/n^- junction to a profile, which is trapezoidal in shape and peaking both at p^+/n^- junction and n^-/n^+ junction. Though the field builds up at the n^+/n^- junction, it does not reach the critical field to cause avalanche injection at this junction. The generation of free carriers and their transport

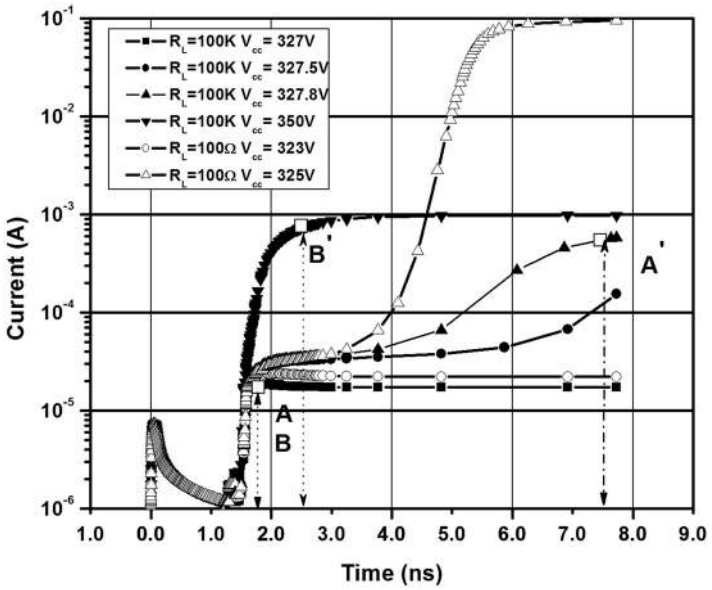

FIG. 9. Current buildup across a $p/n^-/n^+$ structure ($N_D^+=10^{18}/\text{cm}^3$, $N_D^-=10^{15}/\text{cm}^3$, and $N_A^+=10^{19}/\text{cm}^3$; $L_{A+}=5$ μm, $N_D\sim 10^{15}$, $L_{D-}=18$ μm, and $L_{D+}=2$ μm) (with reference to Fig. 5) when a voltage is ramped to the values indicated in 1.55 ns under different load conditions.

causes redistribution of the electric field, causing oscillatory behavior between $t=1400$ ps and $t=2100$ ps, as generated carriers modulate the electric field in the depletion region, though not enough to cause avalanche injection.

However, if the load resistance is reduced to $R_L=100$ kΩ, as shown in Fig. 6, the modulated electric field across the n^+/n^- junction becomes sufficiently large to cause avalanche injection at this junction. Due to the positive feedback nature of this mechanism, there is more accumulation of carriers, triggering the regenerative mechanism, which eventually leads to snapback phenomenon. The propagation of the avalanche multiplication over the area of the p/n^- junction was investigated for different ramping conditions and it was observed that fields higher than the breakdown field can be achieved across the junction only if the voltage is ramped quicker than $\sim$150 ps.

In Figs. 7 and 8, the spatial distribution of electron and hole concentrations, impact generation rate, and electron current densities are plotted at different times for loads of $R_L=10$ MΩ and 100 kΩ, respectively. The electron distributions [shown in Fig. 7(a)] show that the carriers move from the p/n^- junction (where they are generated), and accumulate in the n^- region. However, the hole concentration [shown in Fig. 7(b)] rises slightly in the n^- region, causing the field to rise at the n^-/n^+ junction. Thus the impact generation rate [shown in Fig. 7(c)] peaks at the n^-/n^+ junction (at $t=1450$ ps) and settles to a lower steady-state value as the electric field falls, preventing the sustained avalanche injection at the n^-/n^+ junction from causing second breakdown of the device. Figure 8 shows the results when the load resistance was reduced to $R_L=100$ kΩ to aid the avalanche injection across the n^-/n^+ junction. The redistributed electric field is strong enough to sustain impact ionization [shown in Fig. 8(c)] at both junctions at $t=1480$ ps. As the electron and hole concentrations rise [shown in Figs. 8(a) and 8(b)] the oscillatory behavior due to the transit-time effect is more prominent (compared to Fig. 7) due to the greater generation rate [shown in Fig. 8(c)] at both junctions. Modulations in electron current densities for both the breakdown conditions are shown in Figs. 7(d) and 8(d). After the regenerative double injection phenomenon is triggered the change in electric field at the n^-/n^+ junction is relatively slow (beyond $t=2000$ ps). Figure 9 shows the buildup of the diode current as a function of time when the voltage is ramped to different levels in about 1500 ps. The figure shows a sharp rise in current (which shows the triggering of double injection mechanism) for a slight variation in the final ramp voltage for different values of load resistance R_L. The device exhibits a sudden jump in the current when the final ramped voltage is varied from 327.5 to 327.8 V when the load resistance is $R_L=100$ kΩ. There is a delay of a few nanoseconds before the sharp increase in current as the double injection phenomenon takes place. However, after the initial sharp rise in the current shown in the figure, the device shows a slow increase in current as indicated by AA′ when the final ramp voltage is 327.8 V (delay is $\sim$6 ns). However, this delay is drastically reduced when the voltage is ramped to 350 V in 1.5 ns, the delay being subnanosecond as indicated by BB′. When the load resistance is reduced to $R_L=10$ kΩ, the two different breakdown states occur in the voltage range of 324–325 V. When the load resistance is further reduced to 100 Ω, the transitional range remains 324–325 V.

Since the processes of (a) impact ionization, (b) increase in electron concentration and resulting current density, and (c) redistribution of electric field are highly coupled, the cumulative process is nonlinear and the associated delays in the process are very sensitive to the boundary conditions, explaining the large variation in the delay associated with the onset of second breakdown in Fig. 9. Simulation results also show that shortening the length of the n^- region leads to a decrease in the voltage where the transition region occurs. When $L_{D-}=20$ μm, the voltage where the transition occurs is $V_t=335$ V and at $L_{D-}=16$ μm, $V_t=316$ V.

B. Erratic Behavior

Second breakdown can be interpreted as current-controlled behavior of the avalanche generated current. The

electric-field buildup at the n^-/n^+ junction is related to the current density in the n^-/n^+ junction region. The increased ramp speed leads to greater current density at the n^-/n^+ junction and results in conditions in which second breakdown is more probable. The current density needs to change by only a small amount to create the critical breakdown electric field at the n^-/n^+ junction, triggering the regenerative process that leads to greater probability of second breakdown.

The erratic nature of the second breakdown can be explained due to the extremely sensitive nature of the build up of breakdown field at n^-/n^+ junction to the initial conditions and fluctuations in the voltage ramp rate.

IV. CONCLUSION

Experimental results pertaining to the erratic-mode second breakdown are presented. It is shown that the reverse-biased base-collector junction junction of a BJT undergoes a collapse of voltage when a very fast voltage ramp is applied across it. For an intermediate ramp rate, the device exhibits erratic behavior where it can go into either of two different states. Numerical simulations of the transient response of the voltage ramps applied to symmetrical $p/n^-/n^+$ structures, shows existence of two very close breakdown states. It has been demonstrated that nature of breakdown is very sensitive to the voltage ramp. Faster ramp rates cause more favorable conditions for second breakdown to occur and the erratic nature has been explained due to the complex and coupled nature of the breakdown process and the buildup of electric field due to accumulation of carriers at n^-/n^+ junction.

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