Effect of grain-boundaries on electrical properties of *n*-ZnO:Al/*p*-Si heterojunction diodes

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Mohit Kumar, Aloke Kanjilal, and Tapobrata Som

Effect of grain-boundaries on electrical properties of *n*-ZnO:Al/*p*-Si heterojunction diodes

Mohit Kumar,[1] Aloke Kanjilal,[2] and Tapobrata Som[1,a]
[1]*Institute of Physics, Sachivalaya Marg, Bhubaneswar 751 005, Odisha, India*
[2]*Department of Physics, Shiv Nadar University, Gautam Budh Nagar, Near Greater Noida 203 207, Uttar Pradesh, India*

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We report on room temperature diode characteristics of ZnO:Al (AZO)/Si heterostructures by current-voltage measurements. In this study, with increasing AZO film thickness, systematic reduction in the turn-on potential (from 3.16 to 1.80 V) and the film stress are observed. Complementary capacitance-voltage studies reveal a decreasing trend in barrier height at the junction with increasing AZO film thickness. A gradual decrease in resistivity takes place with increasing AZO film thickness. Above observations are explained in the framework of AZO thickness dependent variation in grain size and in turn trap density at the grain boundaries influencing carrier transport across the adjacent grains. [http://dx.doi.org/10.1063/1.4823480]

I. INTRODUCTION

ZnO is a good candidate for fabricating solar cells,[1] heterojunction diodes,[2] and photodetectors[3] due to its wide band gap, E_g (~3.3 eV), large binding energy (60 meV), and high transparency. Recently, doping of group III elements in ZnO films[4] (especially Al-doping) has also generated considerable interest. For instance, they are not only important for different applications including fabrication of transparent conductive oxide[1,5,6] but also from the fundamental standpoints. However, the thickness dependent optimization of optical and electrical properties of AZO films is essential for photovoltaic and optoelectronic applications, where the carrier concentration dependent resistivity can reach the value as low as 10^{-4} Ωcm,[7] considering the substitution of Zn by Al atoms. Within a moderate Al-doping, it is known that the broadening of E_g is associated with partial filling of states above the conduction band minimum of AZO – known as Burstein-Moss effect,[8] whereas the carrier concentration above the Mott critical density is known to be associated with decreasing E_g due to the modification of the bands through electron-electron and electron-impurity interactions.[9] Different techniques have been employed so far to synthesize AZO films, which includes pulsed laser deposition,[5] chemical processing,[10] direct current (dc) sputtering,[8] etc.

In this paper, we report on the effect of AZO thickness on the current-voltage (*I-V*) and capacitor-voltage *(C-V)* characteristics of *n*-AZO/*p*-Si heterojunction diodes and how the grains are related to it. In fact, we will show systematic reductions in the turn-on potential and the electrical resistivity with increasing AZO film thickness. In order to explain this behaviour, thickness dependent evolution of grains in the deposited AZO films was investigated by atomic force microscopy (AFM) and scanning electron microscopy (SEM), while their nature of crystallinity was examined by x-ray diffraction (XRD).

[a]Electronic mail: tsom@iopb.res.in

II. EXPERIMENTAL

AZO films were deposited on ultrasonically cleaned *p*-type Si(100) wafers (with its native oxide) at room temperature (RT) using a pulsed dc magnetron sputtering system (Excel Instruments). Commercially available 99.99% pure AZO target (50.8 mm dia × 6.35 mm thick, composed of 98 wt.% ZnO and 2 wt.% Al) from Testbourne Ltd., England was used for depositing AZO thin films in a vacuum chamber with a base pressure of $\sim 3 \times 10^{-7}$ mbar. Ultra-pure (99.999%) argon gas was injected into the chamber with a flow rate of 27 sccm to maintain the working chamber pressure of 5×10^{-3} mbar during sputtering. A dc power of 100 W (frequency = 150 kHz, reverse time = 0.4 μs) was supplied (Advanced Energy, Pinnacle Plus) to the AZO target and the substrate was rotated with a speed of 3 rpm for achieving uniform film thickness, where the target-to-substrate distance was 8 cm. The deposition was carried out at an optimized angle of 50° with respect to the target normal.

Four AZO thin films were deposited for 5, 10, 20, and 30 min with an average deposition rate of 6.2 nm/min on Si wafers (diced into small pieces of 1×1 cm^2), named as S1, S2, S3, and S4, respectively. The corresponding thicknesses were measured to be about 30, 70, 120, and 175 nm, respectively within the instrumental error bar, using a surface profilometer (Ambios, XP-200). Many films were deposited to check the uniformity in thickness value before making the devices. Phase identification and crystalline orientation were investigated by XRD (Bruker, D8 Advance) using a Cu-K_α radiation ($\lambda = 0.154$ nm) over a 2θ scan range of 20–60°. Surface morphology was examined by *ex-situ* AFM (Asylum Research, MFP3D) in tapping mode. For each sample, several images were taken from different regions to check the uniformity and to estimate the average grain size and root mean square (rms) roughness. In addition, the deposition time dependent evolution of grains in AZO films was monitored by SEM (Carl Zeiss) in both plan-view and cross-sectional geometries using 5 keV electrons. Silver paste was used to make electrical contacts on the top of AZO films and the back side of the Si substrates. The formation of Ag/AZO/Si/Ag heterostructure diodes was verified by taking *I-V* characteristics using an electrometer (Keithley, 6517A) based resistivity measurement setup. The junction barrier height was investigated by performing capacitance-voltage (*C-V*) measurements at a frequency of 1 MHz using HP 4284A precision LCR meter.

III. RESULTS AND DISCUSSION

Figures 1(a) and 1(b) show AFM images of S1 and S4 samples, exhibiting a gradual change in surface morphology with increasing deposition time. It appears that the average grain size increases with deposition time (prominent in S4). The average grain size was measured to be 22, 26, 32, and 36 nm for S1, S2, S3, and S4, respectively (all images are not shown). One can also see a clear colour change on the surface (using a camera) with increasing thickness (photographs shown below the AFM images of S1 and S2) and can be explained in the framework of strain-induced variation in the band gap with increasing AZO film thickness.[11] On the other hand, the rms surface roughness is found to increase monotonically with increasing film thickness (Table I). Besides investigating the thickness variation of the AZO films as a function of deposition time by SEM in cross-sectional geometry, we have seen the formation of elongated grains — tightly packed and aligned normal to the Si surface. Typical plan-view and cross-sectional SEM images of S3 are shown in Figure 2.

The XRD patterns of S1-S4 shown in Figure 3 confirm the formation of crystalline grains. The dominant peak located around 34.1° can be attributed to the (002) reflection from the hexagonal wurtzite structure,[8] indicating the formation of highly oriented grains along the *c*-axis. Formation of the preferentially oriented AZO (along the *c*-axis) grains suggests that the value of the surface free energy is minimum for the AZO (002) plane at the growth stage.[12] As the film thickness increases, the (002) peak intensity is found to increase systematically with a continuous decrease in full width at half maximum (FWHM), signifying the evolution of bigger grains with deposition time up to 30 min. The average grain size was determined for all four samples S1-S4 using Scherer's formula:[8] $D = 0.9\lambda/\beta cos\theta$ where D is the crystallite size, β is the FWHM, θ is the Bragg's angle, and λ is the x-ray wavelength (Table I). From the table, one can see that the measured grain sizes from AFM are little bigger than the ones derived from XRD data. This is because of the limitation of

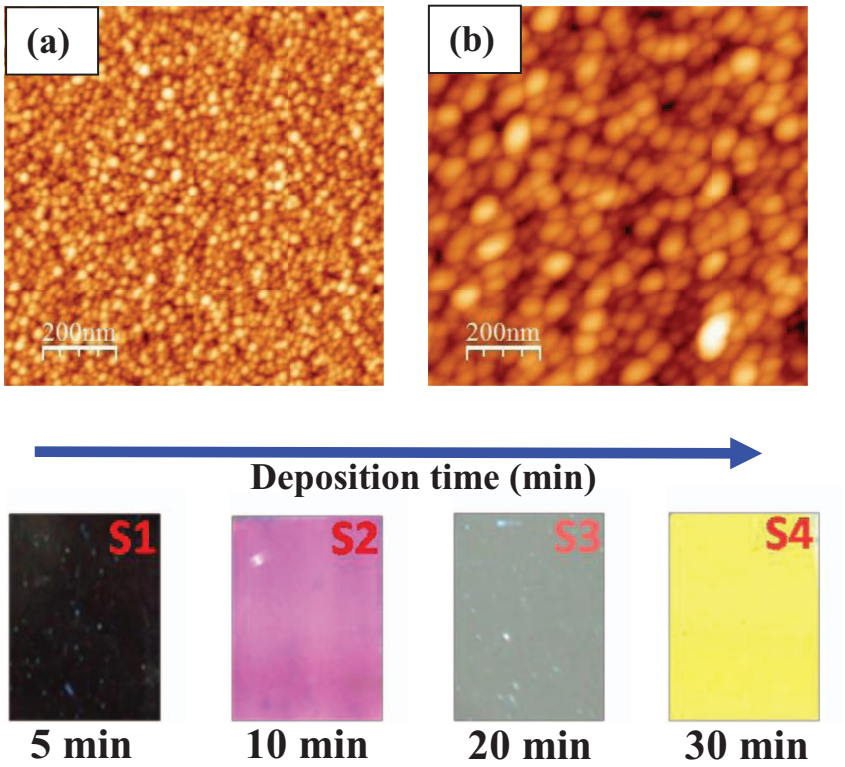

FIG. 1. AFM micrographs ($1\mu m \times 1\mu m$) of AZO films deposited on Si: (a) S1 and (b) S4 with height scales of 6.3 nm and 22.18 nm, respectively. S1 to S4 are the original photographs of the films deposited for 5 min, 10 min, 20 min, and 30 min, respectively.

TABLE I. Following parameters were determined for the AZO/Si hetrostructures in S1 to S4: rms surface roughness (nm), and average grain size (nm) from AFM; peak position (2θ), FWHM (deg), average grain size (nm), strain (%), and stress (Nm^{-2}) from XRD; turn-on potential (V), series resistance (kΩ), and ideality factor from *I-V* characteristics. Negative signs in strain and stress values indicate their compressive nature.

	AFM		XRD					I-V		
Sample No.	rms surface roughness (nm)	Av. grain size (nm)	Peak position (2θ in deg)	FWHM (deg)	Av. grain size (nm)	Strain (%)	Stress (σ in 10^9 Nm^{-2})	Turn-on potential (V)	Series resistance (kΩ)	Ideality factor (n)
S1 (5 min)	0.63	22	34.06	0.53	17	−0.98	−4.27	3.26	7.5	1.7
S2 (10 min)	1.19	26	34.07	0.44	21	−0.93	−4.18	2.65	7.4	1.7
S3 (20 min)	2.32	32	34.10	0.37	26	−0.91	−4.13	2.25	7.2	2.4
S4 (30 min)	2.78	36	34.14	0.32	30	−0.90	−4.06	1.80	6.1	2.7

AFM to resolve smaller crystallites within a bigger grain.[13] In addition, a systematic shift in the (002) peak position was observed with increasing AZO layer thickness. It is known that peak shift toward a lower 2θ value with respect to the bulk pure and doped ZnO films can be attributed to compressive stress in the films originating from oxygen implantation during the sputtering process.[11] In-plane film stress was calculated on the basis of biaxial strain model: $\sigma = [2C_{13}\text{-}C_{33}(C_{11}+C_{12})/C_{13}] \times (c\text{-}c_0)/c_0$ where elastic stiffness constants are: $C_{11} = 2.1 \times 10^{11}$ Nm^{-2}, $C_{33} = 2.1 \times 10^{11}$ Nm^{-2}, $C_{12} = 1.2 \times 10^{11}$ Nm^{-2}, and $C_{13} = 1.05 \times 10^{11}$ Nm^{-2}.[8,11,14] After putting the above values, σ becomes -4.5×10^{11} $(c\text{-}c_0)/c_0$ Nm^{-2}. For a hexagonal lattice with (002) orientation, $c = 2d_s$ and $c_0 = 2d_0 = 0.5206$ nm where d_s is the inter-planar spacing derived from the (002) peak position

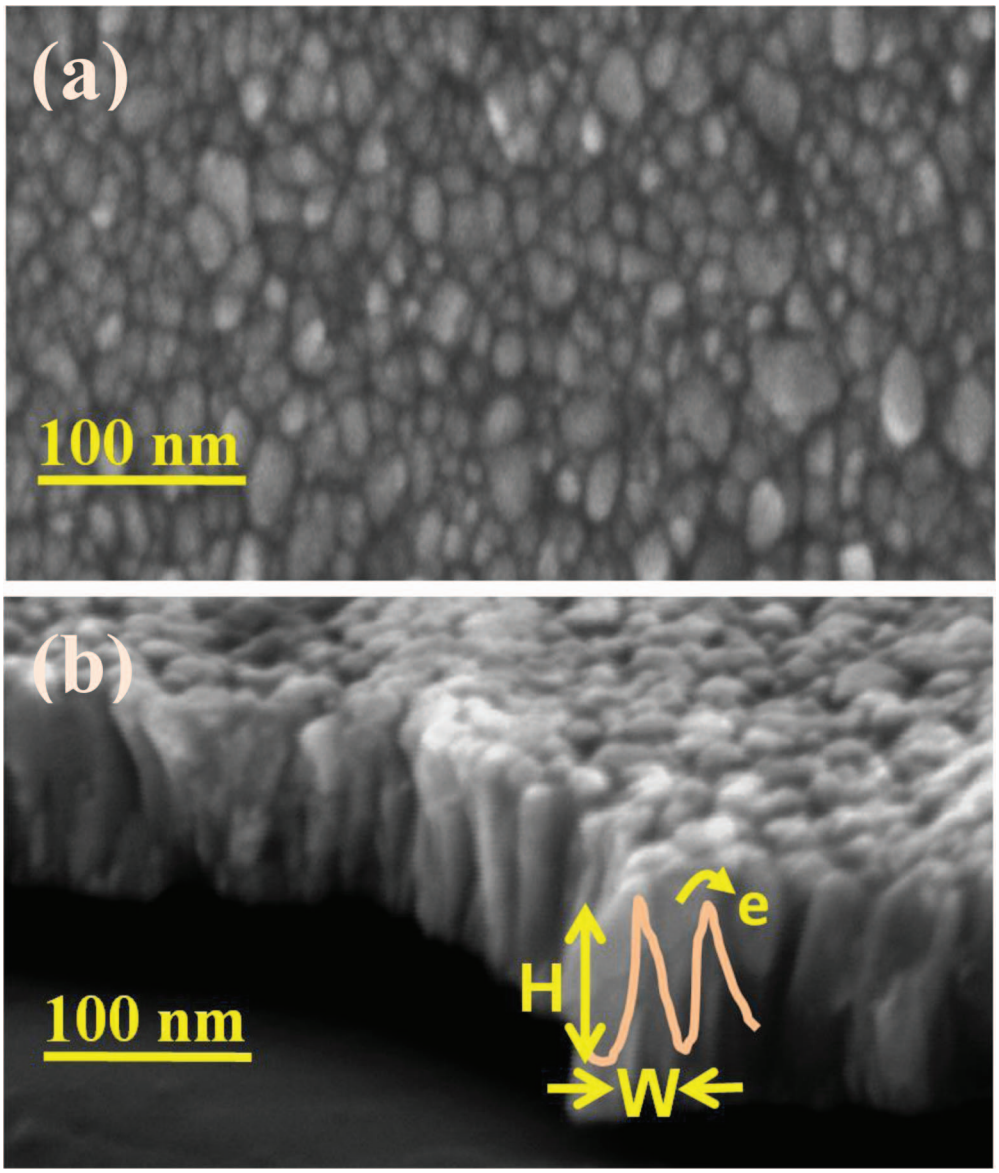

FIG. 2. (a) Plan-view and (b) cross-sectional SEM images of S3 sample. Charge transport across potential barriers (shown by line profile) at grain boundaries is shown schematically on cross-sectional SEM image.

(Figure 3) and d_0 is the corresponding one for stress-free system (0.2603 nm).[15] Accordingly the calculated stress values for S1 to S4 are presented in Table I which reveals that the AZO films become relaxed with increasing thickness – in accordance with Ref. 11. From the above discussion one can derive the film strain using the relation:[15] $[(d_s - d_0)/d_0] \times 100\%$ which are summarized in Table I.

For resistivity measurements, we used the AZO films grown on commercial glass slides simultaneously and under similar conditions as on Si substrates. Figure 4 shows the thickness dependent variation of resistivity measured by linear four-probe technique. A sharp decrease in resistivity was recorded for S1 to S2, whereas it remained almost constant for S3 and S4. Note that, the linear variation of the *I-V* characteristics (inset, Figure 4) of AZO films on glass substrates confirms the Ohmic nature of the silver contacts. On the other hand, the *I-V* characteristics of all Ag/AZO/Si/Ag heterojunction diodes [Figure 5(a)] show the rectifying property where schematic view of such a diode is depicted in the inset (bottom corner). The diode series resistance and the ideality factor can

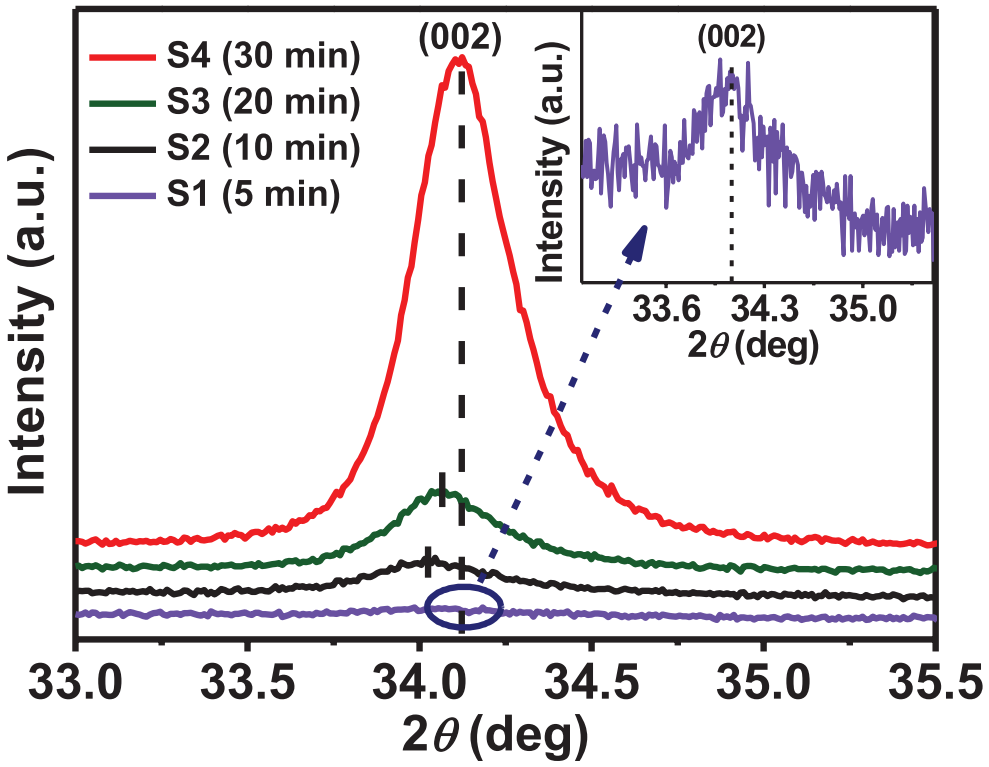

FIG. 3. Thickness-dependent XRD patterns. For a better projection the magnified region around the (002) reflection of S1 is shown as the inset.

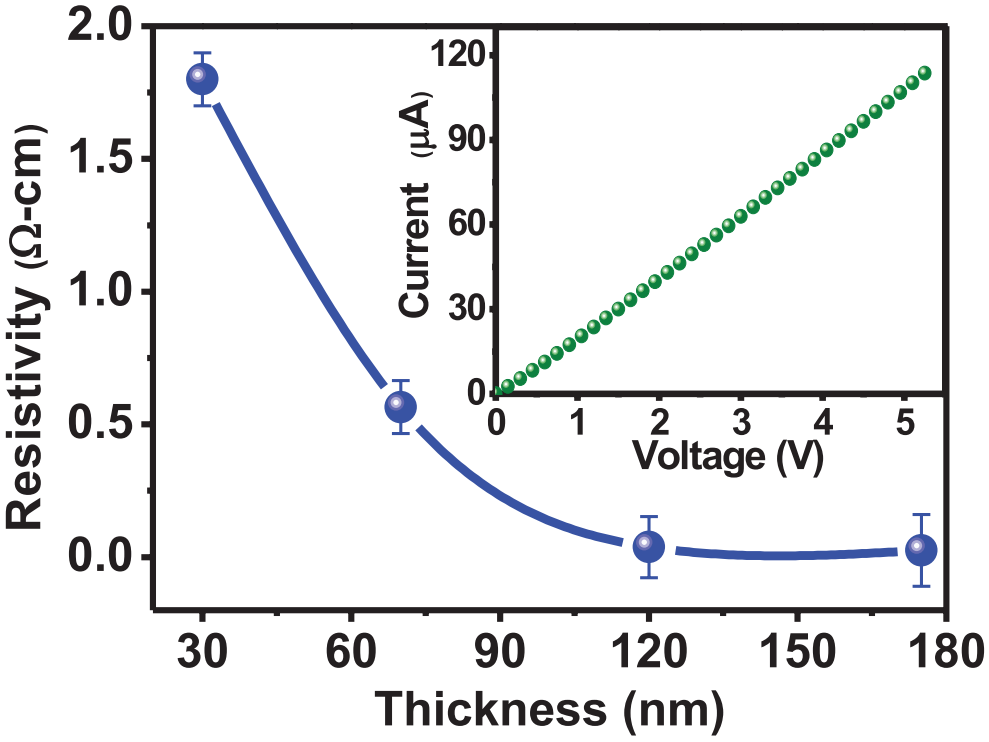

FIG. 4. Variation in resistivity with AZO film thickness. Inset shows the linear variation of current with applied voltage corresponding to the silver contacts.

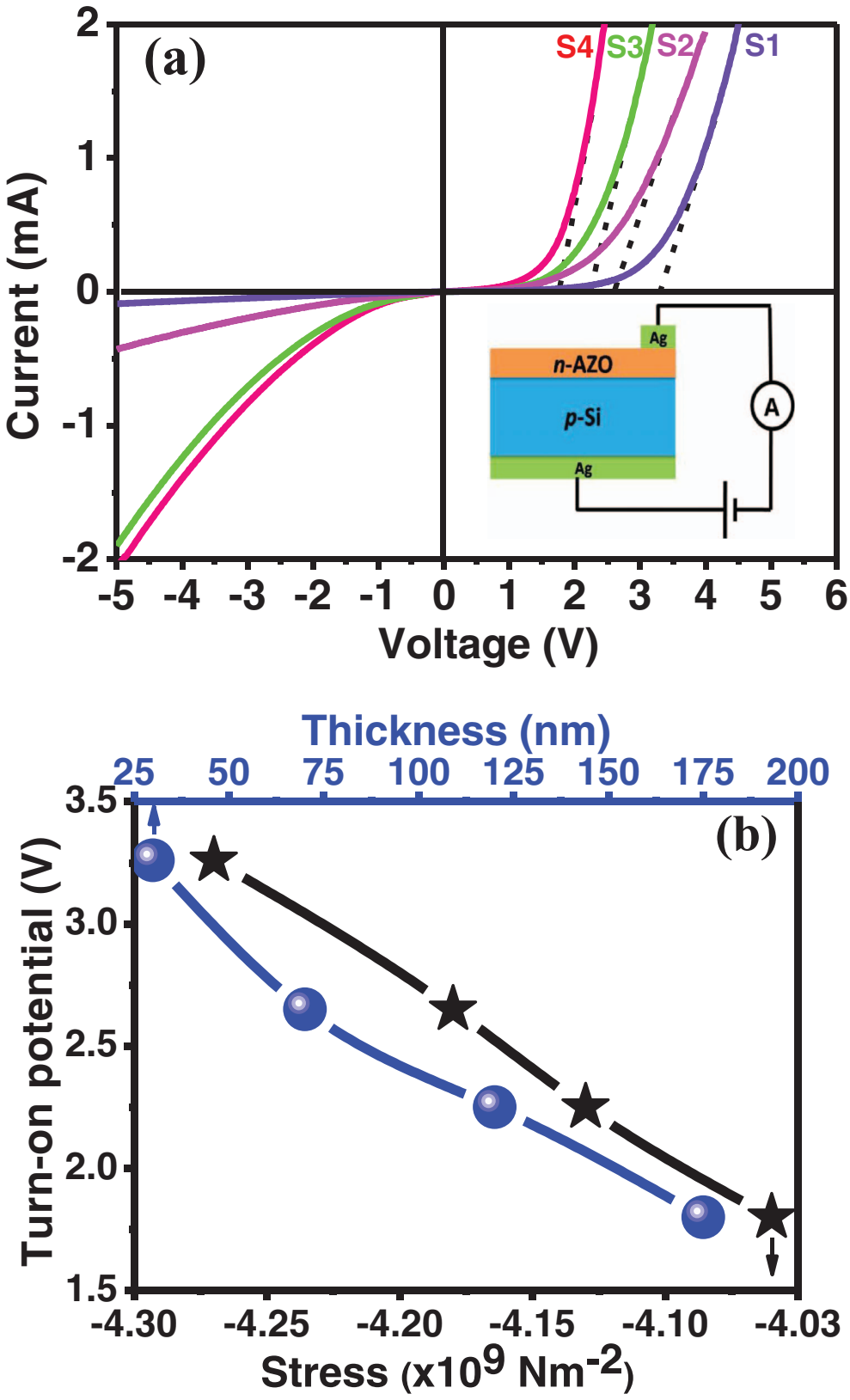

FIG. 5. (a) Thickness dependent nonlinear *I-V* characteristics of all AZO/Si hetrojunction diodes (shown schematically in the bottom inset), (b) variations in turn-on potential with AZO thickness and film stress.

be obtained from[16] $dV/d(ln\ I) = [IR_s + nk_{BT}/q]$ where V is the applied potential, I is the measured current, R_s is the series resistance, n is the diode ideality factor, k_B is the Boltzmann constant, T is the sample temperature, and q is the electrical charge. The calculated values of n and R_s from the slope and the intercept at zero voltage in the ln I versus V plot (not shown) are summarized in Table I.

Because of having a large lattice mismatch between the AZO layer and Si(100) substrate,[6] dislocations appearing at the AZO/Si interface can lead to the increase in ideality factor, n (Table I). As the AZO/Si interface plays an important role in carrier injection, we believe that the AZO thickness dependent increase in n is most likely associated with the minority carrier injection and recombination.[17] This is consistent with the increase in reverse saturation current (I_0) with increasing AZO film thickness, which in turn takes part in suppressing turn-on potential by decreasing the barrier height, ϕ_B at the AZO/Si interface [Figure 5(a)]. The barrier height ϕ_B at a temperature of T can be determined from $I_0 = A^*ST^2\exp(-\phi_B/k_BT)$, where S is the surface area of the diode, k_B is the Boltzman constant, and A^* is the Richardson constant.[18] Since we cannot avoid the presence of a thin native SiO_x between the AZO layer and the Si substrate, the extracted ϕ_B will be erroneous due to the active participation of AZO/SiO_x and SiO_x/Si interfaces, especially for thin AZO layers with thicknesses below 70 nm [see the reverse current profiles in Figure 5(a)]. This is because of incorporation of a large amount of defects between the AZO/SiO_x and SiO_x/Si interfaces which as a result can contribute in charge transfer process between the AZO film and the Si substrate.[19,20]

In order to determine ϕ_B, we did C-V measurements at 1 MHz under a forward and reverse bias sweep of 4 to −4V. For applied voltage $V \gg k_{BT}/q$ and $N_A \gg N_D$, the capacitance per unit area can be written as $1/C^2 = 2(V_{bi}-V)/q\varepsilon_s N_D$ where the N_A and N_D are the donor density in n-AZO and the acceptor density in p-Si, respectively; V_{bi} is the built-in potential within Si, and ε_s is the Si permittivity.[18] Using $1/C^2$-V plot (Figure 6, shown for S1 and S3 for clarity) the extrapolated straight line intercept of $1/C^2$ on V axis is the measure of ϕ_B.[21] The AZO film thickness dependent change in ϕ_B is displayed in the inset of Figure 6, showing a systematic decrease in ϕ_B from 0.9 to 0.3 V with increasing thickness up to 175 nm. From the above results it can be inferred that the AZO/Si heterojunction diode characteristics, especially the turn-on potential is strongly influenced by the growth of AZO films and their thicknesses.

Different theoretical models have been proposed so far to explain the electrical properties of the AZO/Si hetrojunction diodes where the most acceptable one is the bandgap model with and without SiO_2 layer.[2,3] Earlier band alignment and the microstructure of the ZnO/Si hetrojunctions were studied in detail and used to explain the nonlinear behaviour.[3] In the present scenario, the notable decrease in the turn-on potential with increasing AZO film thickness [Figure 5(b)] can be described in light of decreasing stress. In fact, we have seen strain relaxation with increasing AZO thickness (Table I), which is possibly due to the increase in grain size. The presence of traps at the AZO grain boundary and their impact on transmission of electrons (or holes) have recently been demonstrated by scanning tunnelling microscopy.[22] Based on this concept, it is now possible to explain the observed phenomena in the framework of defect-induced potential barrier formation at the grain boundaries, while the magnitude of the barrier height (H) and width (W) are associated with the trap density between two adjacent grains [shown schematically in Figure 2 where the line profile represents the potential (due to traps) at grain boundaries]. This in turn controls the charge transport between two grains: the conduction will be increased with reducing H and vice versa. Clearly, the boundary traps dominate in S1 compared to the samples like S2 to S4 due to decrease in surface-to-volume ratio with increasing grain size (Table I).

Although the trap density is reduced with increasing grain size, the decrease in ϕ_B as a function of AZO thickness (discussed above) can enhance the minority carrier injection in inversion through the reduction of depletion width.[17] As a matter of fact, the probability of minority carrier recombination will be increased with increasing AZO film thickness, leading to an increase in magnitude of I_0 by suppressing R_s (Table I). However, considering the existence of a thin native SiO_x between the AZO layer and the Si substrate, the minority carrier injection may be influenced by degree of tunnelling through surface states.[23] Hence, the diode characteristics degraded with increasing AZO layer thickness. On the other hand, with increasing grains as a function of AZO

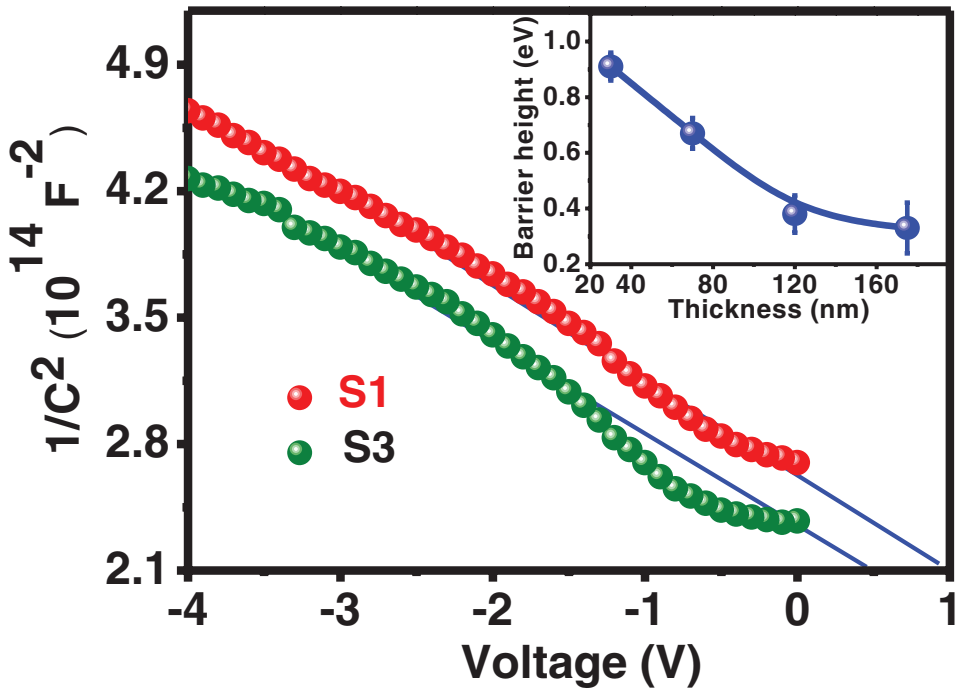

FIG. 6. Typical $1/C^2$-V characteristics for S1 and S3, where the inset depicts the variation of barrier height as a function of AZO film thickness.

layer thickness can increase the mean free path of electrons. In fact, the energy of electrons with increasing AZO film thickness will be conserved with long mean free path,[24] which in turn will reduce the scattering loss[25,26] and trapping of charge carriers, resulting in a decrease in resistivity (Figure 4).

IV. CONCLUSION

In conclusion, the variation in grain size with increasing *n*-AZO film thickness on *p*-type Si(100) substrates was shown by AFM, whereas the XRD results confirm the enhancement of (002)-oriented crystalline grains. Thickness dependent reduction of compressive stress was also demonstrated by XRD measurements. Further, we observed the rectifying property of AZO/Si heterojunction diodes from the recorded *I*-*V* characteristics, where the turn-on voltage undergoes a hitherto unseen systematic reduction with increasing AZO film thickness. Using four-probe technique, a systematic decrease in resistivity was found with increasing AZO film thickness. These phenomena have been modelled based on the thickness dependent variation in grain size and in turn trap density at the grain boundaries influencing the charge transport across the adjacent grains. In particular, the development of potential barrier at the grain boundary followed by the scattering of charge carriers were shown to be the controlling factors of the observed *I*-*V* characteristics. The barrier height at the junction, calculated from the *C*-*V* measurements, shows a decreasing trend with increasing AZO film thickness which corroborates well with the observed thickness-dependent behaviour of turn-on voltage of the heterojunction diodes. Such studies would have tremendous impact in development of next generation silicon thin film solar cells[27] and UV detectors.[28]

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