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PAPER

Bipolar effects in snapback mechanism in advanced n-FET transistors under high current stress conditions

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Abstract

This work models high current snapback behavior in n-FET transistors with bottom body contact under high current stress at the drain for ZRAM (Zero capacitor RAM). We analyze 2D current flow in n-FET near the pinch-off region and relate the results to the S-shaped snapback characteristics under high injection avalanche generated carriers conditions. The role of surface bipolar effects on the first snapback phenomenon in the GG-NMOS (Gate-Grounded NMOS) is investigated. A novel physical insight of the bipolar activity is modeled through current flow and barrier lowering at the source-substrate junctions. Moreover, the coupling of electron and hole injection is described. Finally, a model for surface potential inside the substrate before and after snapback is derived and compared with TCAD simulation results. A very good agreement is observed between the model and the TCAD results.

1. Introduction

Physics of ZRAM is based on parasitic bipolar formation in advanced nano-meter scaled FET transistors. As we go to post CMOS era, ZRAM is a critical device for memory circuit in microprocessors. The lack of clear understanding of the bipolar physics has lead to inaccurate model development for a critical feature of sanpback memories. However, the first snapback behavior is not clearly understood [1, 2]. Figure 1 shows the schematic of a GG-NMOSFET, along with its I-V characteristics, when a current ramp is applied at the drain terminal. The snapback behavior in such devices is primarily related to the bipolar turn-on mechanism [3]. However, the electrostatic coupling between source(S), drain (D) and gate terminals has not been clearly addressed.

In the body of NMOSFET bipolar turn on is taking place which is causing snapback as shown in figure 2, where source terminal is behaving like emitter of the BJT, drain terminal is behaving like collector of the BJT and body or substrate is behaving as base of the BJT. Sufficiently large voltage across the collector and base causing impact ionization, with some of the generated carriers then acting as the initiating current as they flow into the base. Once this initiating current flows into the base, the transistor turns on and the collector voltage decreases to the snapback holding voltage shown in current voltage characteristic section of figure 1. This voltage happens at the point where the processes of base current generation and the bipolar transistor turning on are in balance. The collector-emitter current of the bipolar transistor decreases the collector voltage, resulting in a lower electric field. It leads to a smaller impact ionization or avalanche current and thus smaller base current, which weakens the bipolar action.

Traditionally in an NMOS, lateral parasitic bipolar turn-on mechanism under snapback has been described by crowding of electrons, which is manifested as the base push-out/Kirk effect [3–7]. The critical electrostatics of hole crowding near 'pinch-off' has been overlooked [8]. Moreover, potential build-up due to 2-D current flow in the n-FET devices, so far lacks clear physical insight [9]. Earlier work involves studying the effects of different parameters on bipolar turn-on mechanisms [10–12], but the critical electrostatics of different regions of the NMOSFET under high current stressed condition and their mutual coupling are often overlooked. Also accurate

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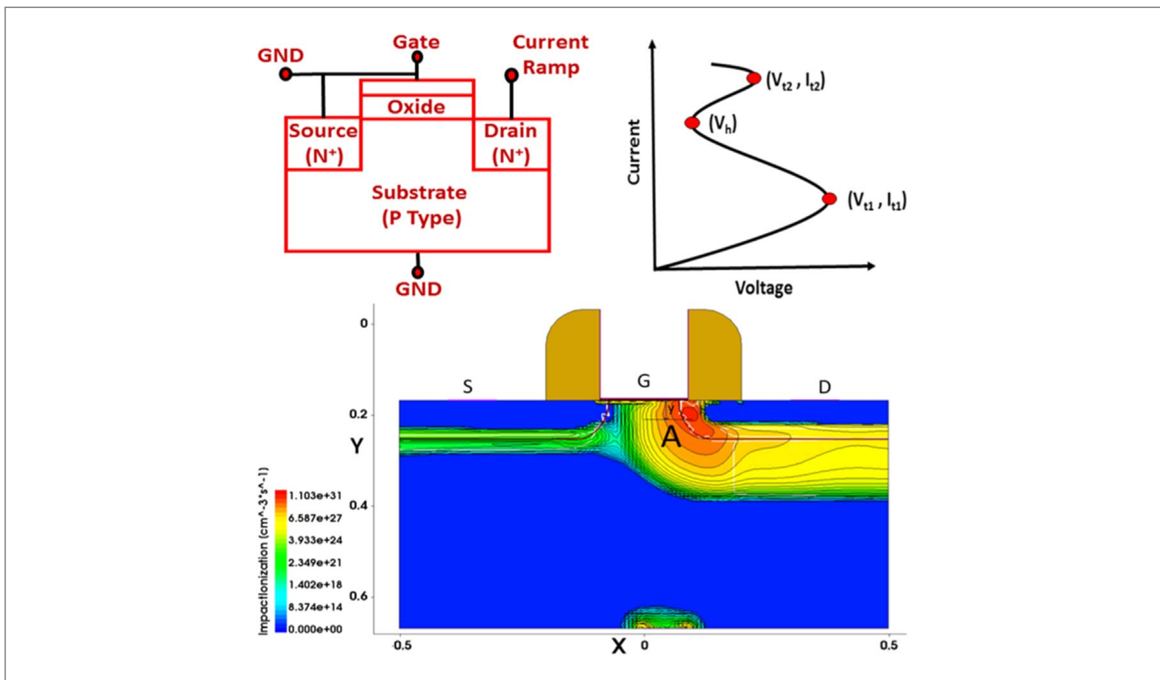

Figure 1. Schematic of GG-NMOS and I-V characteristics when current ramp is applied at drain contact. MOS structure with source and gate electrostatics coupling along with boundary conditions. Point A is the high electric field point in simulated device.

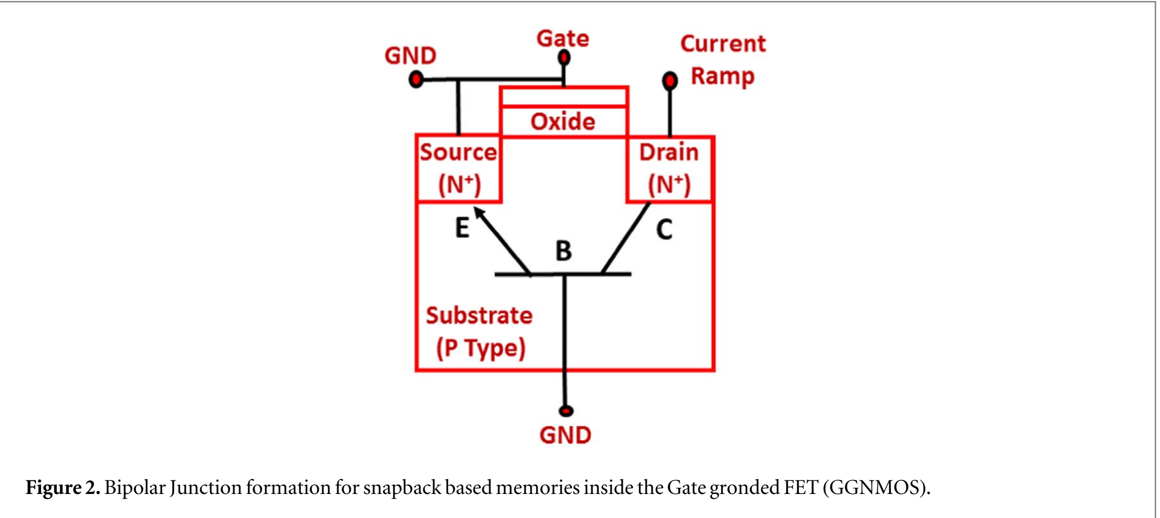

Figure 2. Bipolar Junction formation for snapback based memories inside the Gate gronded FET (GGNMOS).

modeling of important parameters such as (V_{t1}; I_{t1}), V_h and (V_{t2}; I_{t2}) is more involved [13–18]. In this work, we describe the fundamental mechanisms of current flow in the 2D-FET, based on the microscopic features of snapback and the impact of 2D current flow, which determines the I-V characteristics. The analysis is critical in understanding the nano-meter scale n-FET structures under high current conditions. Moreover,the translation of these TCAD models into CAD environments for building circuit simulation models will be useful for the circuit designer. In this article, we report snap-back features during bipolar turn-on and model the high current injection phenomenon. In section 2, we describe the process of snapback and surface bipolar activity using two-dimensional TCAD simulations under high current stress conditions. The crowding of holes at the drain contact and the injection of holes in the substrate and coupling with the source region is discussed. In section 3, analytical models of the surface potential is derived for the bulk region. TCAD result is compared to the derived analytical expression in section 4. Finally, the mutual dependence and coupling of the source and drain are analyzed.

2. 2D device simulation and physics of high current injection

The structure of the GG-NMOS transistor used in the study is shown in figure 1. The 2D device characteristics were simulated using the Sentaurus TCAD device simulator with default parameter coefficients. Here, We

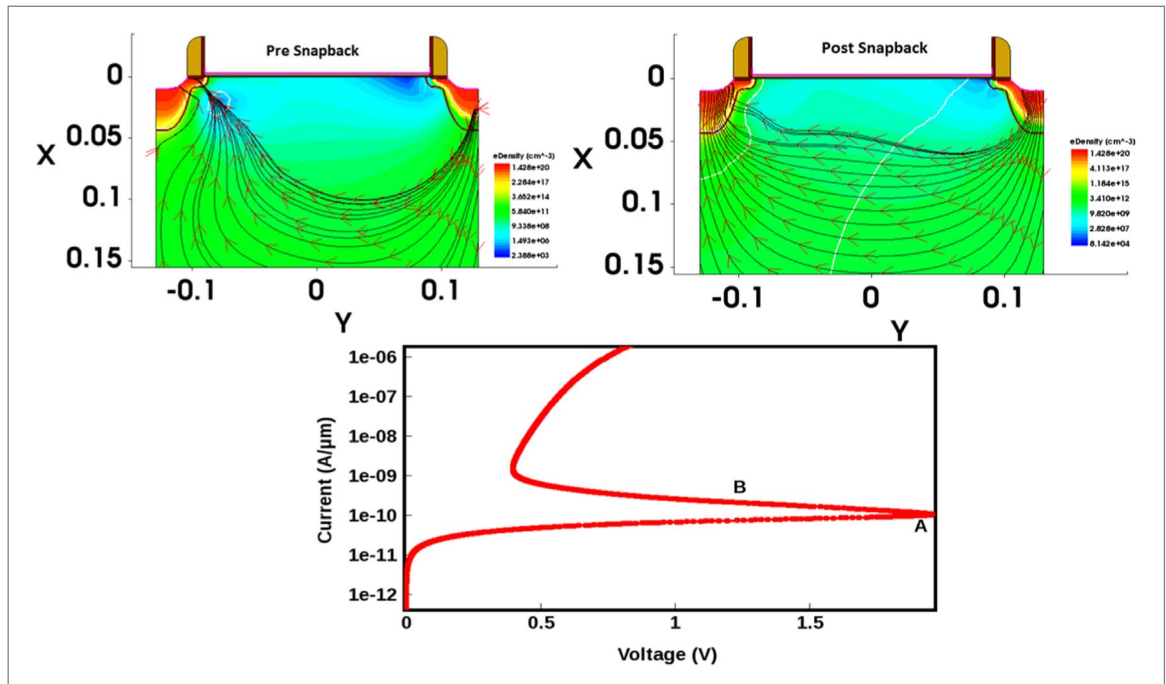

Figure 3. I-V characteristics showing snap-back (Point 'A' Pre Snapback and Point 'B' Post snapback) for the device structure. Current flow lines showing Pre Snapback and Post Snapack in simulated 2D structures.

performed 2D transient device simulations and investigated the mechanisms of snapback under high current injection, when a current ramp is applied to the drain contact. In the simulations, the current ramp is adjusted to study the dependence of snapback on the rise time of the pulse.

The application of a current ramp to the drain terminal of the GG-NMOS causes the electric field to increase in the drain-bulk depletion region. Avalanche breakdown is triggered at the p/n^{-} junction (shown in figure 1), which results in avalanche-generated holes moving towards the bulk region and avalanche-generated electrons being collected by the drain terminal. Impact ionization peak is maximum at A, where the electric field is highest due to the space charge of the mobile carriers. Figure 3 shows pre and post snapback flow lines indicating Post snapback current flowlines smoothen when recombination current dominates. Whereas, Point A in I-V characteristic related to the 2-D structure showing pre snapback flow lines and point B post snapback flow lines in figure 3. The space charge of the mobile carriers pushes the carriers across the drain contact, where they accumulate - (shown in the band diagram of figure 4). The flow of holes across the substrate influences the barrier height on the source side, primarily within the bulk (SB) region, while the gate region is more or less shielded from the influence of the flow of holes flowing towards the substrate. Moreover, the space charge due to holes are initially imaged by the bulk contact towards the bottom. Thus injected excess holes are not imaged on the source side due to coulombic shielding (see figure 4(a)). Furthermore, the hole accumulation at the drain-bulk junction increases the perturbation in electric field and change in barrier height is observed, exhibiting the coupling between the source and bulk regions. The coupling can also be understood through the potential variation in the bulk region as shown in figure 4(b) in a 2D device structure. Thus, due to establishment of the electric field, holes can start flowing towards the bulk contact and the hole-current density increases in the bulk region which is visible in the (contour profile) buildup of hole in figure 4(a). Hole injection into the substrate leads to perturbation of potential (as shown in the figure 4(b) and in the process leads to electron injection below the surface. Now electron injection from the source end leads to compensation of space charge due to holes and in the process triggers snapback as shown in the figure 4(c). Since the drain-bulk depletion region is under the influence of space charge limited (SCL) transport, it acts as a current-controlled two dimensional SCL resistor and exhibits a ballast action due to hole crowding, which leads to potential build-up across the p/n^{-} junction and influences the electric field in the bulk region (figure 4). Moreover, the hole ballast action due to excess hole current shows a linear characteristic and it is worth noting that in the absence of avalanche-generated holes, the voltage drop is entirely across the depleted junction.

2.1. Diffusing injected minority carriers across the surface

From the above discussion, we observe two dimensional electrostatic coupling between the source and bulk, as excess holes are injected from the drain junction. However, the crowded mobile charges are imaged primarily by the bulk contact; thus, the bands bend in the y-direction (see figure 4 band diagram). As the hole injection

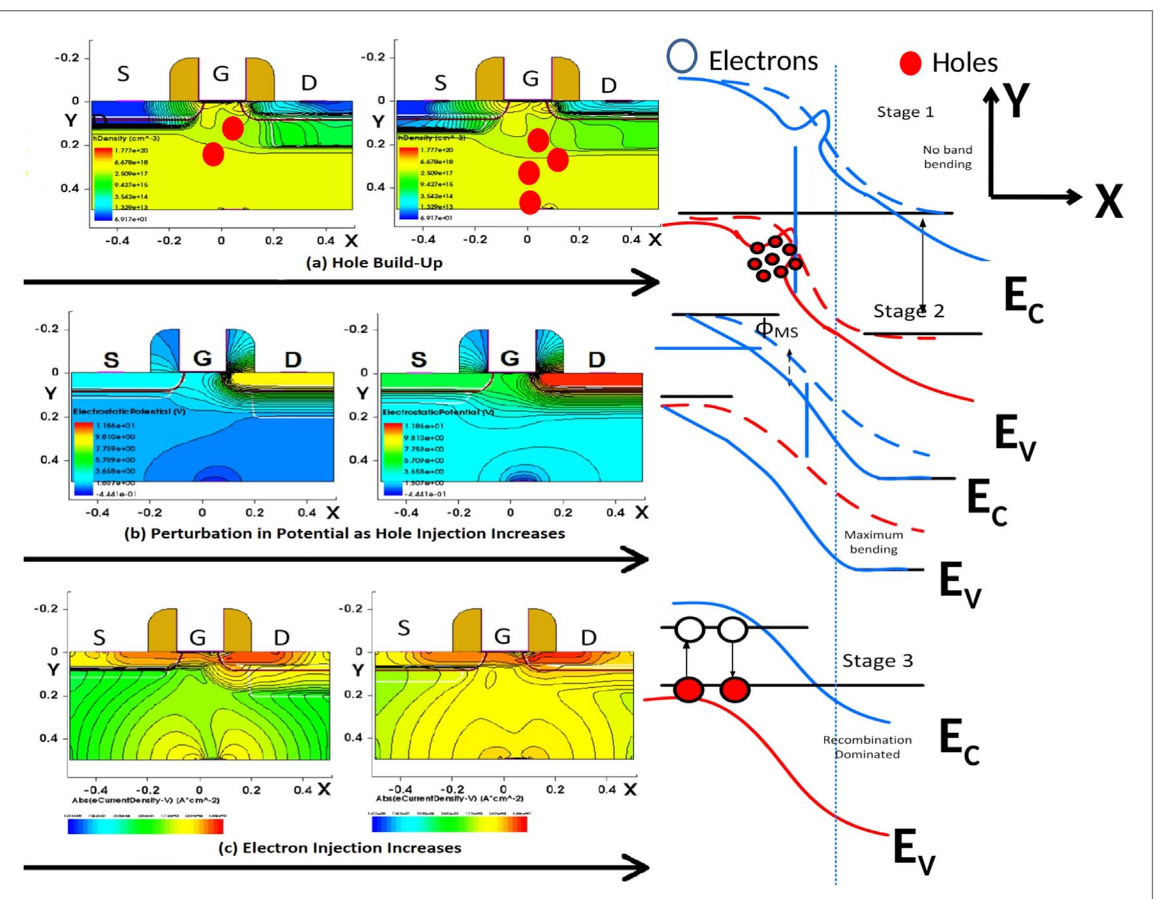

Figure 4. Hole Build-up after impact ionization triggers at Drain-Substrate Boundary (a) Hole Current Density (b) Potential Build-up as hole injection increases. (c) Increase in electron injection from source side as barrier reduction takes place because of increase in hole injection.

becomes stronger, it also perturbs the potential in the x-direction. The barrier to the minority carriers (i.e., electrons) near the source is determined both by the electrostatic coupling of the gate and the substrate with the source, which leads to injection of electrons into the channel below the oxide.

(1) Bulk injected electrons on the source side reduce the width of the depleted channel. The holes accumulate on the drain side.

(2) Initially, in the absence of any injection from the source, diffusion of carriers dominates. In order for the drift to be dominant the band bending in the semiconductor should increase continuously towards the drain side. In the absence of constant gate voltage along the channel, the band bending in the oxide has to decrease by the same amount.

(3) In order to decrease the oxide voltage, the surface injected charges should decrease faster than the depletion charge.

(4) Therefore, the change in band bending in the semiconductor and the oxide is negligible as one approaches the drain.

(5) However, it is not possible because the device is far away from weak inversion region (in absence of gate potential). The maximum voltage drop in the channel is much less than ϕ_F, which keeps the entire channel away from weak inversion.

(6) The combination of very small voltage drop in the channel, coupled with the small charge in the weak inversion layer, makes drift current negligibly small in the channel.

Therefore, one can observe that in the absence of gate bias the injected carriers primarily diffuse below the oxide in the bulk and even if sufficient holes are injected from the drain region (large barrier lowering), the diffusion component remains dominant. However, During the entire cycle of bipolar turn-on mechanism, the first

snapback behavior is observed. The simulated results show complete bipolar turn-on process and a potential build-up as injection of hole increases and therefore injection of electron from source side, as shown in figure 4.

2.2. Salient features of surface and bulk bipolar turn-on & bipolar gain of the device

Current injection from the source end is maximum across the bulk, where not only the barrier height is minimum but also the base transport factor is maximum as shown in figure 4.

(1) However, the minority electrons are swept across the surface where initially the electrons are attracted to the depleted channel.

(2) Now, the carrier gradient is maximum primarily because the electron concentration is maximum along the surface and slowly the carrier concentration increases towards drain. Thus the carriers which are injected in the bulk are swept along the surface. As the bipolar injection increases, the surface carriers efficiently shield the injected bulk electrons and in the process they begin to flow in the bulk.

(3) Similarly, towards the drain side, holes accumulate near the surface, shielding the gate from attracting holes, which prefer to stay below the gate on the right side.To summarize, injected electrons accumulate along the surface from the source end and holes accumulate from the drain end. Slowly, the substrate below the gate attains neutrality and injected electrons begin to flow in the bulk. As the bipolar structure turns on, the activity slowly shifts to the bulk where the injection has started at first and the recombination is maximum. Once excess carrier build-up stops, the voltage buildup stops and one can clearly observe the onset of negative resistance, which is taken as the point where the device begins to filament first in 2D and subsequently 3D.

(4) The current injection is maximum in the bulk. However, electrons are swept along the surface where the gradient is maximum. Now the carrier gradient is maximum primarily because the electron concentration is maximum at the surface.

(5) Where it was assumed that the semiconductor is non-degenerate and that the difference between the electron and hole quasi Fermi energies in electron volt equals the applied voltage in volt. High injection of carriers causes to violate one of the approximations made in the derivation of the ideal diode characteristics, namely that the majority carrier density equals the thermal equilibrium value. Excess carriers will dominate the electron and hole concentration and can be expressed in the following way.

$$n_p p_n = n_i^2 e^{\frac{V_a}{V_t}} \tag{1}$$

$$n_p = \frac{-n_i^2 e_b^{\frac{v_a}{v_b}} + \sqrt{n_i^2 e_b^{\frac{v_a}{v_b}} + 4N_a}}{2} \approx \sqrt{N_a}\sqrt{\frac{n_i^2 e_b^{\frac{v_a}{v_b}}}{4N_a} + 1} \tag{2}$$

3. Analytical modeling

The schematic cross section of the GG-NMOS transistor is shown in figure 5, where L is the length of the channel and W is the width of the device. To develop the analytical model for the first snapback mechanism in the n-FET devices, we described the surface bipolar turn-on mechanism. The device is divided into three regions: (i) source region (ii) drain region, and (iii) bulk region. The carrier injection electrostatics are summarized in figure 4, showing the nature of the potential distribution, along with the flow of holes and electrons in the bulk region. The coupled electrostatics of the drain and bulk can be determined by the amount of hole and electron injection in the bulk region. In order to determine the potential distribution in the bulk region, a cubic polynomial expression for potential is taken as an approximation.

Poisson's equation in the bulk region is:

$$\frac{\partial^2\psi(x, y)}{\partial x^2} + \frac{\partial^2\psi(x, y)}{\partial y^2} = -\frac{J_T}{\epsilon_{Si} V_{Sat}} \tag{3}$$

where, $\psi(x, y)$ is the electrostatic potential in the channel region, ϵ_{Si} is the permittivity of silicon, $J_T = J_E + J_H$ is the total injected hole and electron current density in the bulk, and V_{Sat} is the saturation velocity. The potential variation inside the MOSFET can be approximated by the cubic polynomial potential function as described in [19]

$$\psi(x, y) = a_0(x) + a_1(x)y + a_2(x)y^2 + a_3(x)y^3 \tag{4}$$

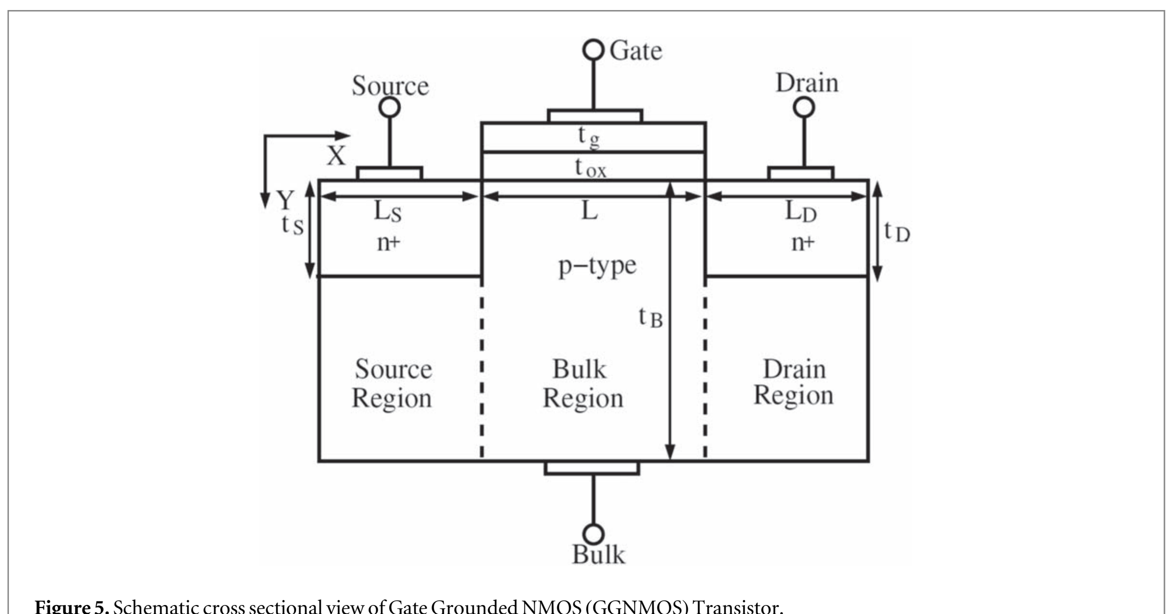

Figure 5. Schematic cross sectional view of Gate Grounded NMOS (GGNMOS) Transistor.

The coefficients $a_0(x)$, $a_1(x)$, $a_2(x)$, and $a_3(x)$ are functions of x only. To find these coefficients, we use the boundary conditions as mentioned below.

(1) The electric displacement at the silicon body/gate oxide interface is continuous.

$$\left.\frac{\partial\psi(x, y)}{\partial y}\right|_{x=0} = \frac{\epsilon_{ox}}{\epsilon_{Si}} \times \frac{\psi_f(x) - (V_G - V_{FB})}{t_{ox}} \tag{5}$$

where, $\psi_f(x)$ is the electrostatic potential at the silicon body/gate oxide interface, ϵ_{ox} represents the gate oxide dielectric constant, t_{ox} is the thickness of the gate oxide layer, V_G is the applied gate voltage and V_{FB} is the flat band voltage.

(2) The electrostatic potential at the back side of the silicon body is zero since the substrate is grounded.

$$\psi(x, t_b) = 0 \tag{6}$$

(3) The electric field at the back side of the silicon body is zero.

$$\left.\frac{\partial\psi(x, y)}{\partial y}\right|_{y=t_b} = 0 \tag{7}$$

(4) The source end potential is simply the built-in potential V_{bi} between the n-type source and p-type channel since the source is grounded.

$$\psi(x, 0) = V_{bi} \tag{8}$$

(5) The drain end potential is the built-in potential plus the drain bias voltage V_{DS}.

$$\psi(x, L) = V_{bi} + V_{DS} \tag{9}$$

Here, we have assumed an abruptly doped source/drain-to-channel junction and corner effects [20] are neglected.

Now differentiating (4) and substituting the boundary conditions 1 and 2 in it, we can find the values of the coefficients $a_0(x)$, $a_1(x)$ and $a_2(x)$ as

$$a_0(x) = \psi_f(x) \tag{10}$$

$$a_1(x) = \frac{\epsilon_{ox}}{\epsilon_{Si}} \times \frac{\psi_f(x) - (V_G - V_{FB}}{t_{ox}} \tag{11}$$

$$a_2(x) = \frac{3a_1(x) - 2a_2(x)t_b}{t_b^2} \tag{12}$$

$$a_3(x) = \frac{a_2(x)t_b - 2a_1(x)}{t_b^3} \tag{13}$$

3.1. Potential distribution at the surface

Substituting (4) along with the obtained coefficient values in (3) for y = 0, we can get

$$\frac{\partial^2\psi_f(x)}{\partial x^2} - C_{1,f}\psi_f(x) = C_{2,f} \tag{14}$$

The values of $C_{1,f}$ and $C_{2,f}$ are obtained by putting the values of $a_0(x)$, $a_1(x)$, $a_2(x)$, and $a_3(x)$ in (4) and then substituting (4) in the (3) and by setting $y = 0$ for surface of the device,

$$C_{1,f} = \frac{6}{t_b^2} - \frac{4C_{ox}}{t_b\epsilon_{Si}} \tag{15}$$

$$C_{2,f} = -\frac{J_T}{\epsilon_{Si}V_{Sat}} - \frac{4C_{ox}}{t_b\epsilon_{Si}}(V_G - V_{FB}) \tag{16}$$

After solving the above second order differential equation using the boundary conditions (8) and (9), we have the gate-oxide/silicon-body potential distribution:

$$\psi_f(x) = K_{1,f}\exp\left(\sqrt{C_{1,f}}x\right) + K_{2,f}\exp\left(-\sqrt{C_{1,f}}x\right) - \delta \tag{17}$$

where

$$K_{1,f} = \frac{C_{2,f}\left(e^{\sqrt{C_{1,f}}L} - 1\right)}{C_{1,f}\left(e^{2\sqrt{C_{1,f}}L} - 1\right)} + \frac{\left[V_{bi}\left(e^{\sqrt{C_{1,f}}L} - 1\right) + V_{DS}e^{\sqrt{C_{1,f}}L}\right]}{\left(e^{2\sqrt{C_{1,f}}L} - 1\right)} \tag{18}$$

$$K_{2,f} = \frac{C_{2,f}e^{\sqrt{C_{1,f}}L_{ch}}\left(e^{\sqrt{C_{1,f}}L_{ch}} - 1\right)}{C_{1,f}\left(e^{2\sqrt{C_{1,f}}L_{ch}} - 1\right)} + \frac{e^{\sqrt{C_{1,f}}L_{ch}}\left[V_{bi}\left(e^{\sqrt{C_{1,f}}L_{ch}} - 1\right) - V_{DS}\right]}{\left(e^{2\sqrt{C_{1,f}}L_{ch}} - 1\right)} \tag{19}$$

$$\delta = \frac{C_{2,f}}{C_{1,f}} \tag{20}$$

This potential distribution expression has been verified with Sentaurus device simulator results, as shown in figure 6 and very good agreement between the two is found.

3.2. Turn-on mechanism

The electron and hole current density inside the bulk region after bipolar turn-on can be determined by considering the bipolar action of the device. Due to the application of a pulse signal at the drain terminal a hole current will flow toward the substrate contact. This current will increase the the potential inside the bulk region and when a sufficient forward bias is established between source and bulk, electron current from source to drain starts to flow and bipolar turn on may occur. This electron current (I_S) will cause hole current (I_{sub}) to flow from bulk to source and drain current (I_D) to flow from bulk to drain.

$$I_T = I_S + I_D + I_{sub} = 0 \tag{21}$$

where,

$$I_S = I_{oe}[e^{\frac{V_{BE}}{V_T}} - 1] \tag{22}$$

where, I_{oe} is the reverse saturation current due to diffusion of holes in the source of the MOSFET. The hole current I_{sub} is a function of the avalanche multiplication factor 'M' and electron current I_S.

$$I_{sub} = (M - 1)I_S \tag{23}$$

The multiplication factor can be approximated as;

$$M = \frac{1}{1 - \alpha x_d} \tag{24}$$

where $x_d = \sqrt{\frac{2q}{\epsilon_{Si}N_A}(V_{bi} + V_{DS})}$ is the width of the depletion region and α is given as;

$$\alpha = Ae^{-\frac{B}{E}} \tag{25}$$

A and B are the ionization coefficients and E is the electric field in the high field region.

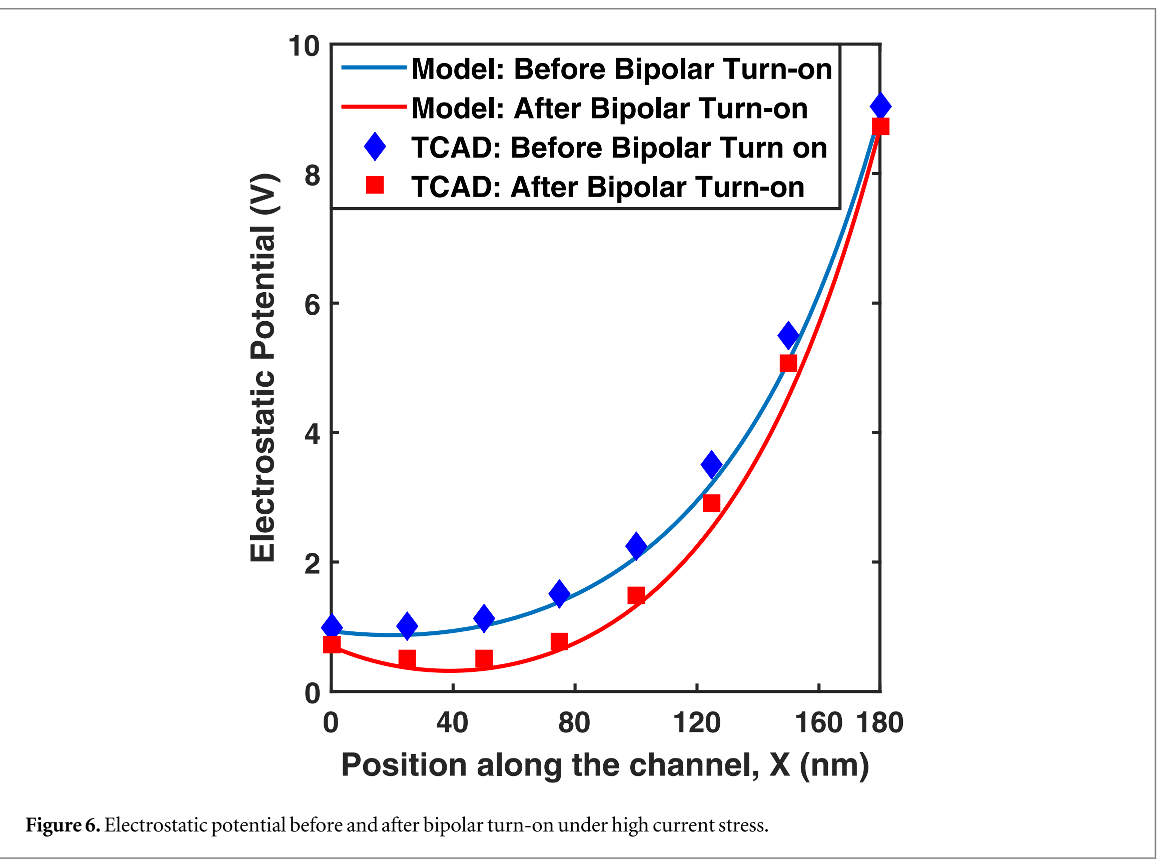

Figure 6. Electrostatic potential before and after bipolar turn-on under high current stress.

4. Conclusions

In this paper, we model the high current ambipolar mechanism of n-FET devices under high current stressing. The formation of bipolar junction within Gate Grounded NFET for snapback based memory (ZRAM) application has been explained. The application of an high current pulse to the drain contact, which results in hole crowding and the injection of holes to the substrate is discussed. Moreover, the coupling mechanism of the drain-substrate junction to the source-substrate junction is modelled and used to explain the bipolar turn-on mechanism. The coupling between electron and hole injection and the electrostatics of different regions of the GG-NMOSFET is discussed.

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